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REALIZATION OF FREQUENCY HOPPING SPREAD SPECTRUM IN HIGH-SPEED WIRELESS COMMUNICATION

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ABSTRACT

The primary goal of designing a digital communication system is to receive data that is identical to the data given by the transmitter. Military communications have frequently employed frequency hopping devices to guard against enemy jamming, interception, and detection. In conventional frequency hopping (FH) systems, the transmitter's pseudo-random code sequence determines the hopping frequency selection, and the receiver responds in precise synchrony with the transmitter's hopping pattern. This study proposes a novel message-driven frequency hopping (MDFH) system to address the ever-increasing demand on information capacity and lessen the strain of synchronization. The hopping frequency selection process may be made to incorporate some information, which can considerably increase the spectral efficiency of the FH system. To show the suggested scheme's higher performance and improved security characteristics, quantitative analysis is performed.

Keywords: MDFH, Xilinx ISE design and Verilog HDL.

I. INTRODUCTION

Due to the rising need for data communication and the fact that digital transmission provides data processing choices not possible with analog transmission, digital communication systems are becoming more and more desirable [2]. A waveform from one of an infinite number of waveform forms with theoretically infinite resolution is sent via an analog communication system. In contrast, a digital communication system (DCS) transmits a waveform over a predetermined length of time from a limited selection of waveforms.

In a DCS, the receiver's goal is to detect which waveform from a restricted set of waveforms was communicated by the transmitter from a confused signal. The simplicity with which digital signals may be created in comparison to analog signals is the main justification for choosing a digital signal. Digital circuits are less prone to distortion and interference than analog circuits are. In order for a binary digital circuit to work in one of just two states—completely on or completely off— A disturbance must be severe enough to shift the circuit's operating point from one state to the other. This two-state approach allows for signal regeneration, avoiding noise and other transmission disturbances.

The conversion of digital symbols into waveforms that are appropriate for the channel requirements is known as digital modulation. These waveforms often take the form of shaped pulses in baseband modulation. When many signals share the same channel, modulation can be employed to differentiate them. The term "frequency-division multiplexing" refers to such a method. In order to lessen the impacts of interference, modulation might be utilized. Spread- spectrum modulation is a subset of these modulation methods that demands a system bandwidth significantly larger than the minimal bandwidth needed by the message.

Frequency hopping was initially developed as one of the two fundamental modulation methods in spread spectrum communications with the intention of being intrinsically secure and dependable for military usage in challenging combat situations. In a traditional FH system, the transmitter uses a pre-specified algorithm to "hop" in a pseudorandom fashion among the available frequencies. The receiver then works in sync with the transmitter and keeps its frequency set to the same center.

In a spread spectrum system, the sent signal is dispersed over a large frequency range—one that is far broader than the minimum bandwidth needed to convey the data being delivered. Spread spectrum communications are not a bandwidth-efficient technology. It does, however, come into its own when used in conjunction with other systems already using the frequency [4].

Narrowband signals and spread spectrum signals can coexist while just slightly raising the noise floor that narrowband receivers experience. Signals in the spread spectrum are "spread" across a large bandwidth. This technology is used to reduce the power density of radio transmissions. Spread spectrum waveforms can also be employed to increase performance, particularly interference tolerance.

We also benefit from spread spectrum's tolerance to frequency-selective fading and rejection of interference or jamming [9]. The capacity to operate in the presence of purposeful or inadvertent interference is one of the most significant benefits of spread spectrum. It can also remove the effects of multipath interference. Unauthorized users or observers are protected via spread spectrum communication.

A well-designed spread spectrum system reduces the capacity of a jammer to interfere by forcing him to guess which communication format is being used.

The intended message is converted to digital form and combined with a pseudo-random noise sequence. This aids in increasing the signal's bandwidth. The resulting words (i.e., digital data) are then serially broadcast after being given a certain frequency (within the available bandwidth).

The information is either jammed or made secret by the transmitted signal and the pseudo random noise only the receiver with the appropriate pseudo random noise can then decode the signal and retrieve the original message.

II. LITERATURE SURVEY

Modeling and performance assessment of a frequency-hopping spread spectrum communication system. In 2010, Yu Zhang et al. developed in Matlab a frequency-hopping system model with BFSK modulation. The system model is made up of a number of components, including a spectrum display, jammer generator, transmitter, receiver, and error rate computation.

The FH/FSK system platform's bit error rate (BER) performance is further analyzed and simulated using noise and narrow-band jamming. Implementation of a Fast Frequency Hopping Spread Spectrum Modulator with System Generator on an FPGA 2009 saw the introduction of a Fast Frequency Hopping Spread Spectrum (FFHSS) transceiver for wireless optical communications by Santiago T. Pérez et al. The brain of the transmitter is a discrete DDS (Direct Digital Synthesizer).

The initial prototype used a PLD (Programmable Logic Device) to create the analog synchronization signal as well as the digital synchronization signal. A separate external filter was also required to remove the high frequency components of the digital synchronization signal. To prevent mixing them with discrete analog circuits, the FFHSS and analog synchronization signals were sent by two distinct optical devices. The goal of this study is to redesign the modulator using System Generator from Xilinx and an FPGA (Field Programmable Gate Array) in order to evaluate the performance of this design technique.

III. ARCHITECTURE OF PROPOSED SYSTEM

Figure 1 show the conversion of the incoming data source into binary digits (bits), which are then gathered to create a digital message. The purpose of source coding is to reduce the amount of bandwidth needed for transmission by eliminating duplication in the transmitted information. The supplied code word is determined by the symbol's probability.

The shorter the code word, the greater the chance. Through the modulation process, message symbols are changed into waveforms that meet the criteria of the transmission channel. The term "baseband" describes a signal whose frequency range starts with a dc component and terminates at a fixed point that is less than a few megahertz. Band pass modulation is necessary for RF transmission applications. Band passing happens when a carrier wave frequency changes the spectral content of a base waveform to a frequency that is significantly higher than the base waveform's spectral content.

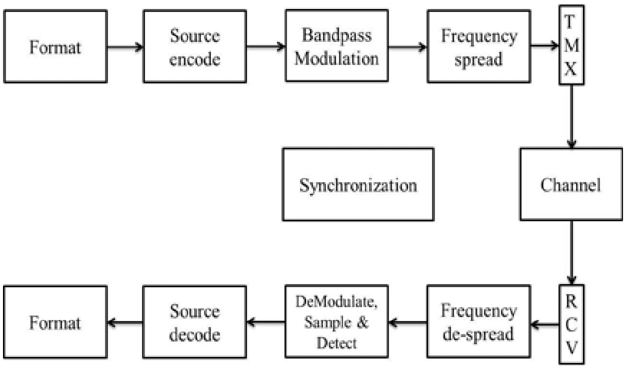


Figure 1: Block diagram of proposed system

DESCRIPTION AND WORKING PRINCIPLE

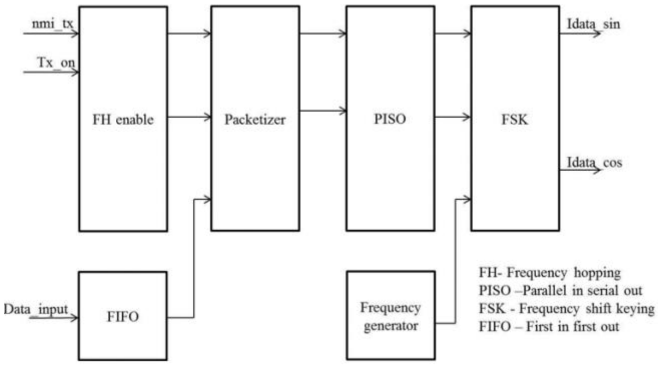


Figure 2: Transmitter block of FHSS system

Transmitter: The high-level block design and flow diagram for the Transmitter that will be utilized and implemented are shown below. The 8-bit parallel prepared data from the test machine comprises source information, destination information, data format, and payload. On the basis of this data, a TX start signal is created. This signal produces two signals: one containing system information (nmi tx) and the other containing payload information. This allows for the two-signal frequency-hopping strategy. Figure 2 illustrates how the payload is isolated from test machine input and serialized to bits using a packetized block.

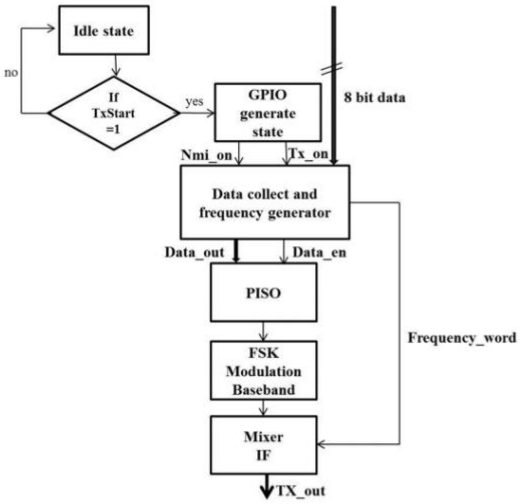
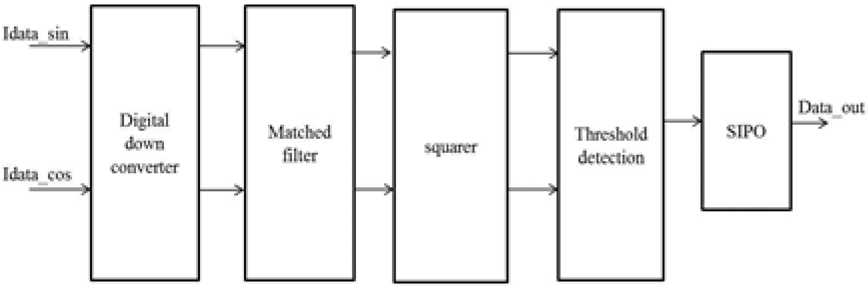


Figure 3. Transmitter flow chart.

Receiver:



SIPO – serial in parallel out

Figure 4.Receiver

Figure 4 depicts the demodulator utilizing correlators. The signal's message and carrier components each have an in-phase and a quadrature component. The input signal is sent to the down conversion block, which multiplies it by the carrier and removes the carrier component using a decimation filter. This filter's output is a baseband frequency component signal that has been downsampled. Then, these signals are routed via correlators filters, which separate the 0 and 1 bit FSK frequencies. The result is then squared to contain only positive values, and a number of samples are averaged to represent a bit.

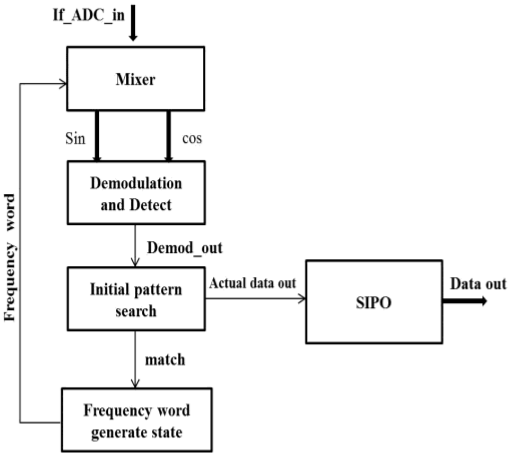


Figure 5: Flow diagram of receiver

IV. RESULTS

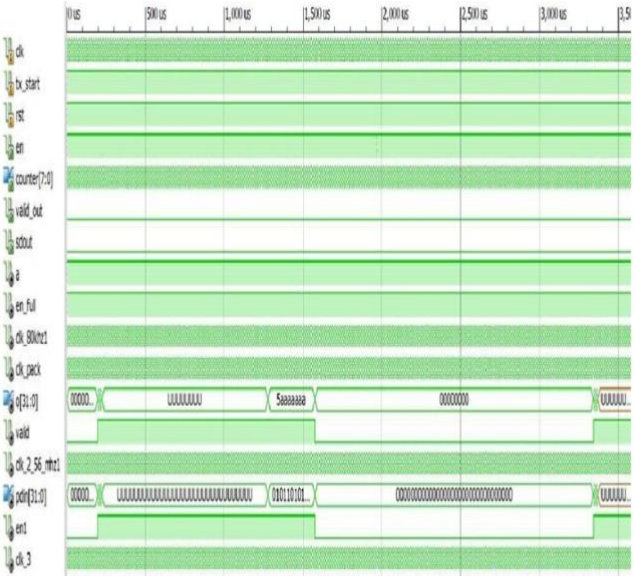


Figure 6: ISim Transmitter Result

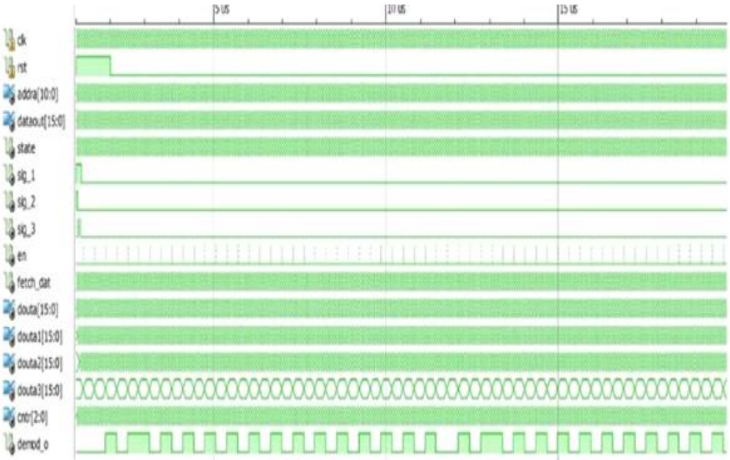


Figure 7. ISim Receiver Result1

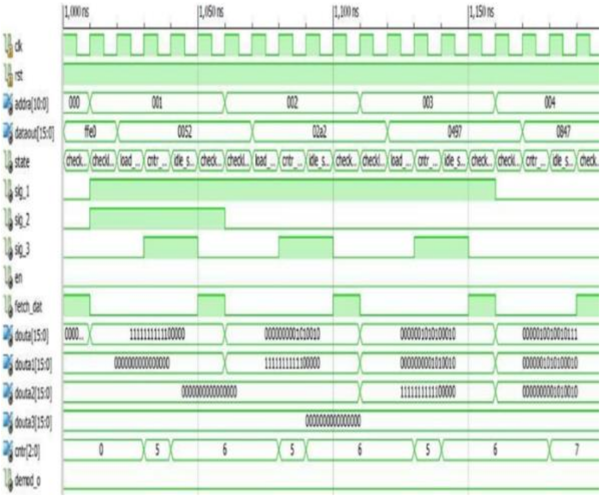


Figure 8: ISim Receiver Result2

V. Result

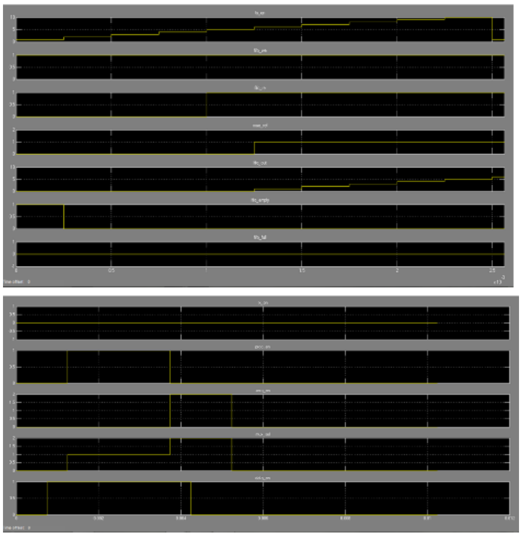


Figure 9: Transmitter Data Enable and FIFO out

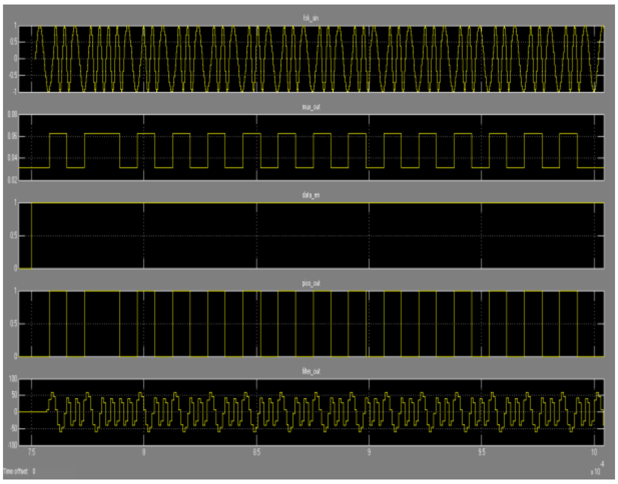


Figure 10: Transmitter filter out with hopping

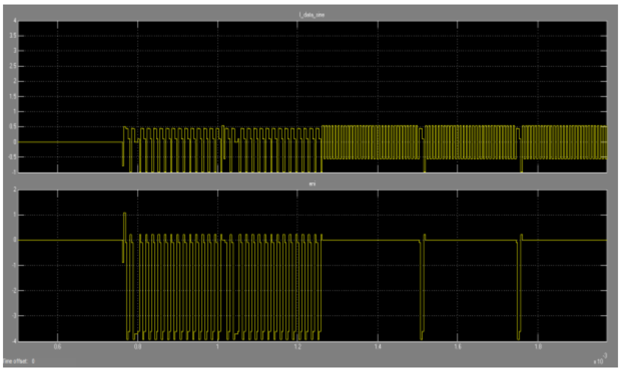


Figure 11: Receiver filter out sine

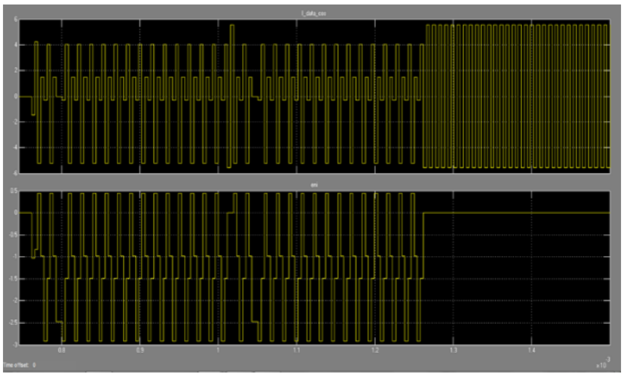


Figure 12: Receiver filter out cos

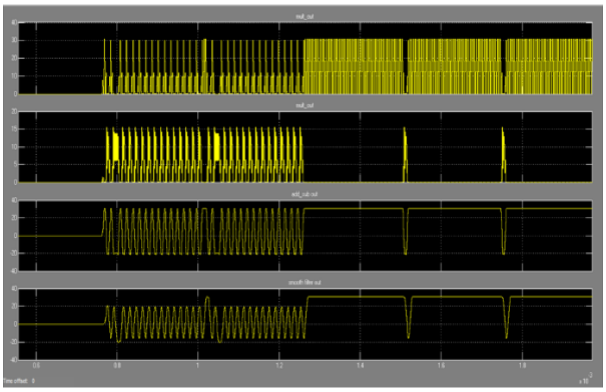


Figure 13: Squarer result

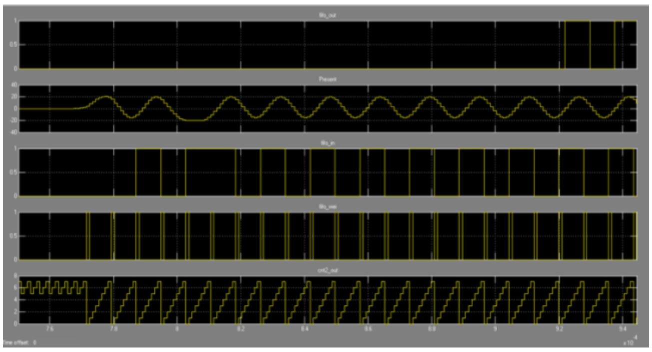


Figure 14: Receiver FIFO out

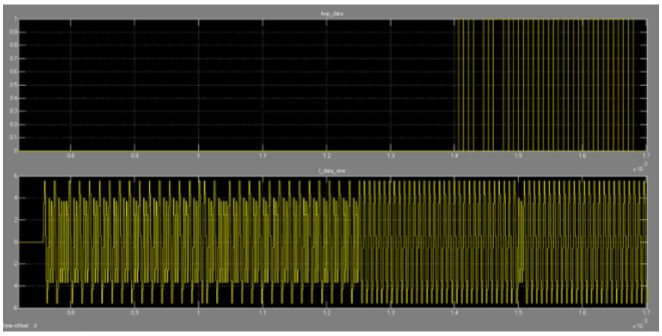


Figure 15: Comparison between I-data_sine and actual hop data

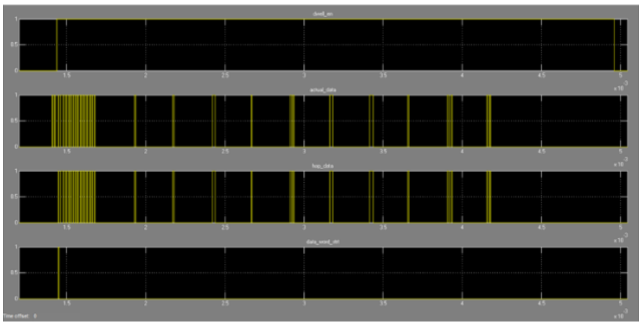


Figure 16: Hop Data result

HARDWARE TESTING RESULTS

Hardware Test Setup

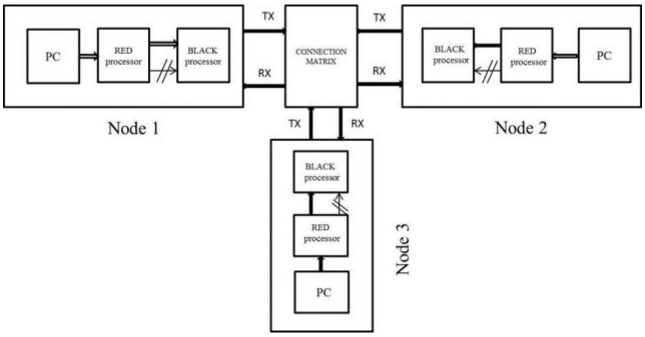


Figure 17: Hardware Test setup

Synthesizable code is provided for Design implementation, as seen in Figures 17 and 18. The Front-End Tool will deliver a synthesized netlist (EDN, NGC) to the Back-End Design Implementation Tools, and we will integrate Placement Constraints through a User Constraints File (UCF). We will also include extra timing and placement limits. Design implementation refers to the process of translating, mapping, placing, routing, and constructing a bit stream file for the design.

BIT files are binary files that contain configuration and proprietary header information. This bit stream file is configured on the FPGA board for hardware testing and displaying the results on an oscilloscope.

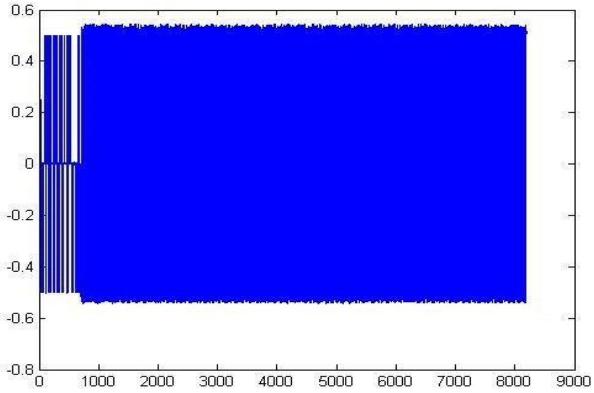


Figure 18: Chipscope Transmitter waveform

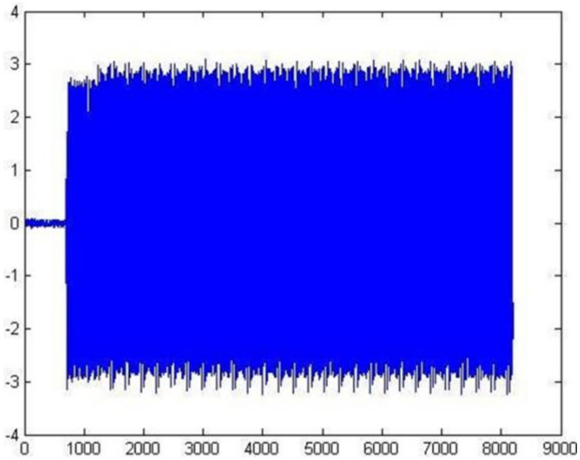


Figure 19:Chipscope Receiver I_Data

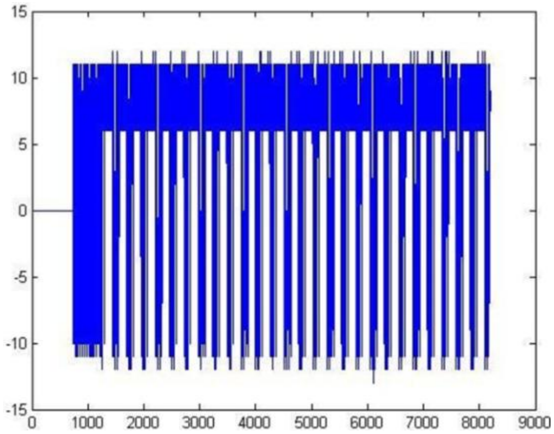


Figure 20:Chipscope Receiver filter out

VI. CONCLUSION

The normal advantages of employing programmable digital devices are realized with this design style. Replicating a design just requires rewriting the FPGA on the board, not creating distinct circuit boards. The alternative prototype improves integration, avoids the need to change analog circuits, and uses fewer external discrete components. The tool's high degree of flexibility makes it possible to quickly test new performance and alter design factors. The signals are shown in floating point format, making it easier to analyze the results of the Simulink simulations since they are simple to conduct. These simulations can be performed before the System Generator blocks are compiled to create the hardware description language files. Verilog and VHDL are the two hardware description languages.

The FHSS and synchronization signals are added in fixed point format in the system developed using System Generator; even a weighted adder can be employed. The adaptability enables modifying the DDS's settings and evaluating its effectiveness. Additionally, it may have an inverse sync filter to account for fluctuations in the sinusoidal signal's amplitude brought on by sampling and retention at the DDS output.

A test model development effort has been done in this project and is made in the baseband processing portion. The high speed FHSS system controllers' integration of Virtex-6 FPGAs has shown certain areas that need to be improved and others that need more research. For various applications with a given data throughput, the hop count may rise. The created model can be included into additional models that can be created as part of an application project.

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