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VALIDATION OF CMOS REVERSIBLE LOGIC GATES AT 16nm REGIME

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ABSTRACT

In ancient times the VLSI technology has demand but in nowadays it has been increased rapidly because of low power consumption, less area is occupied and high speed. In VLSI,CMOS technology was highly preferred because CMOS generates both logic 0 and 1 whereas NMOS generates only logic 1 i.e; VDD and PMOS generates only logic 0 i.e; VSS. By using the VLSI technology the size of the circuits are reducing, the cost of the device reduces, and it has higher reliability. In this paper we use CMOS Reversible gates to maximise the speed, reducing energy consumption and reduces the power dissipation whereas reversible gates consists of Feynman Gate, Peres Gate, Modified Fredkin Gate, Modified Toffoli Gate and Reversible Full Adder using TSG.

I. INTRODUCTION

When the logic operation is being performed on computer's nowadays some of the information is being lost every time . These logic operations are known as "Irreversible Logic". The lost information is being performed inefficiently, and more than kT is dissipating when the every bit is being erased. So, to overcome this limitation Reversible logic gates are being used. While performing the Reversible logic gates operation none of the information is lost and no heat dissipation.

In Reversible logic operations the circuit operates in the backward direction so that the input will be diverting same as that of the output and no power is dissipated. The Reversible logic gates consists of Feynman Gate, Peres Gate, Modified Fredkin Gate, Modified Toffoli Gate and Reversible Full Adder using TSG.

II. PROPOSED SYSTEM

Design and implementation of reversible logic gates using 16nm technology. If we use this method it occupies less area, less power consumption with 50% efficiency and it takes less number of transistors as

Feynman Gate – 12 transistors
Peres Gate – 16 transistors
Modified Fredkin Gate – 18 transistors
Modified Toffoli Gate – 20 transistors
Reversible Full Adder using TSG – 22 transistors

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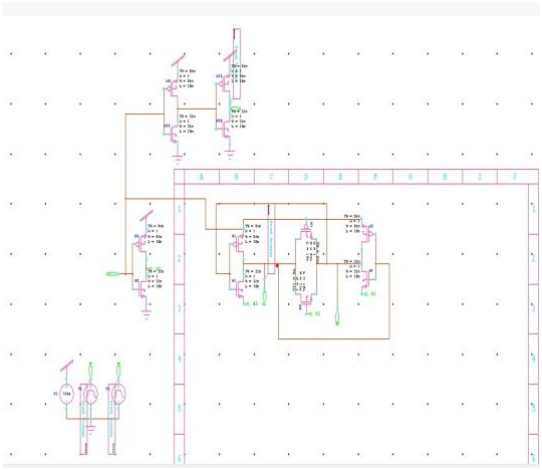


FIG 1: Schematic of Feynman Gate

The above schematic contains the Feynman Gate. The two inputs are A and B. A and B are inputs given to the inverter. Here P and Q are the outputs, A is equals to P and B is equals to A exclusive OR B. To become A is equals to P the Buffer circuit is used. The supply voltage used at V1 is 1.8v. For implementing Feynman Gate 12 transistors are use

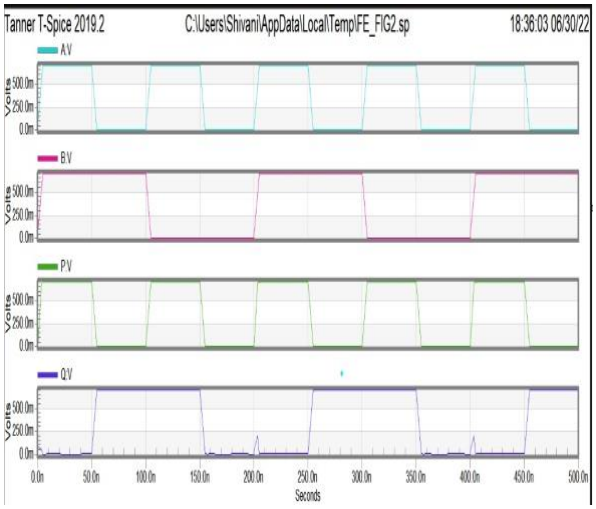


FIG 2: Simulation Output of Feynman Gate

The above schematic shows the Simulation results of Feynman Gate. The inputs are A and B and P and Q are outputs. When input logic A is one and input logic B is one then the output at P is equals to one and output at Q is equals to zero from 0ns to 50ns. When input logic A is zero and input logic B is one then the output at P is equals to zero and output at Q is equals to one from 50ns to 100ns.

When the input logic A is one and input logic B is zero then the output at P is equals to one and output at Q is equals to zero from 100ns to 150ns. When the input logic A is zero and input logic B is zero then the output at P is equals to zero and output at Q is equals to one.

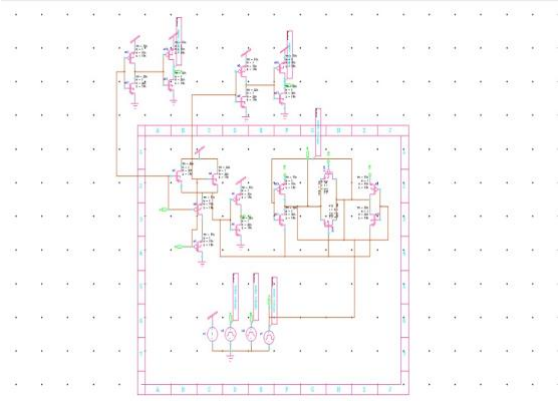


FIG 3: Schematic of Modified Toffoli Gate (MTG) Transistor Level

The above schematic contains the Modified Toffoli Gate (MTG) Transistor Level. It is Reversible gate in the transistor. The two inputs are A and B. Each input is modified by the Reversible gates. Here P,Q and R are the outputs. The supply voltage used at V1 is 1.8v. For implementing Modified Toffoli Gate 20 transistors are used.

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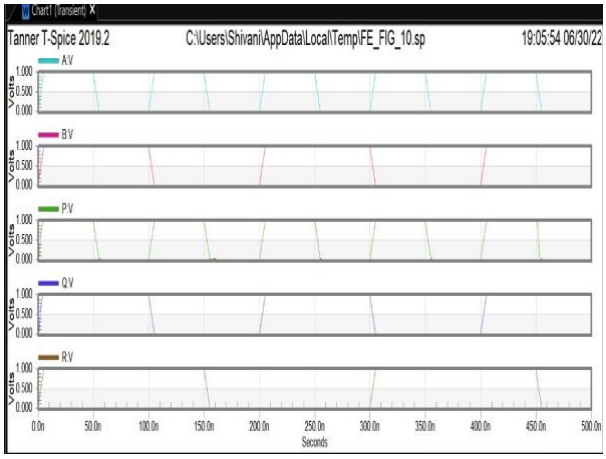


FIG 4: Simulation Output of Modified Toffoli Gate (MTG) Transistor Level

The above schematic shows the Simulation results of Modified Toffoli Gate (MTG) Transistor Level. The inputs are A, B and P,Q and R are outputs. When input logic A is one and input logic B is one then the output at P is equals is one, output at Q is equals to one and the output at R is equals to one from 0ns to 50ns.

When input logic A is zero and input logic B is one then the output at P is equals to zero, output at Q is equals to one and the output at R is equals to one from 50ns to 100ns. When input logic A is one and input logic B is zero then the output at P is equals to one, output at Q is equals to zero and the output at R is equals to one from 100ns to 150ns. When input logic A is zero and input logic B is zero then the output at P is equals to zero, output at Q is equals to zero and the output at R is equals to zero.

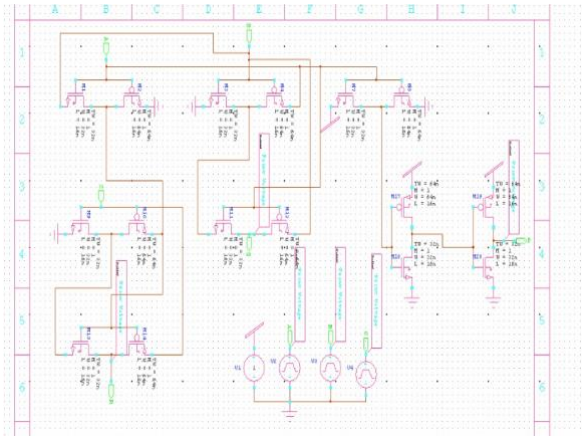


FIG 5: Schematic output of Peres Gate

The above schematic contains the Peres Gate. The three inputs are A,B and C. The inputs A,B and C are fed to the inverter. Here P,Q and R are the outputs, A is given to the inverter to the output of P, B is given to the inverter to the output of Q and c is given to the inverter to the output of R. For implementing Peres Gate 16 transistors are used.

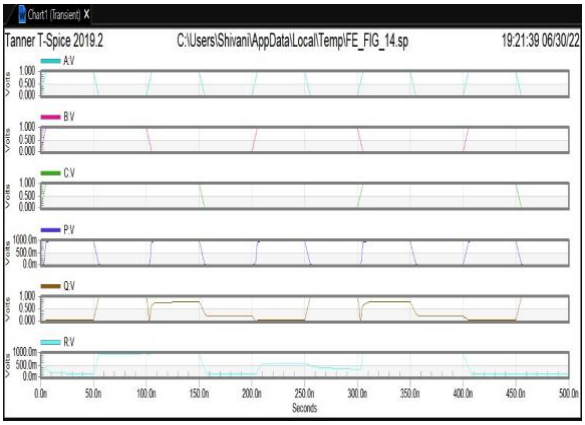


FIG 6: Simulation Output of Peres Gate

Above is Peres Gate's simulation schematic. Inputs A,B,C, outputs P,Q,R. When A, B, and C are all one, P is one, Q is zero, and R is zero from 0ns to 50ns. When A is zero, B is one, and C is one, P is zero, Q is one, and R is one from 50ns to 100ns. When A is one, B is zero, and C is one, P, Q, and R are all one for 100ns to 150ns. When A, B, and C are zero, P, Q, and R are zero from 150ns to 200ns.

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When A, B, and C are one, P is one, Q is zero, and R is zero from 200ns to 250ns. When A is zero, B is one, and C is zero, P is zero, Q is one, and R is zero from 250ns to 300ns. When A is one, B is zero, and C is one, P, Q, and R are all one for 300ns to 350ns. When A, B, and C are all zero, P, Q, and R are all zero for 350 to 400 ns.

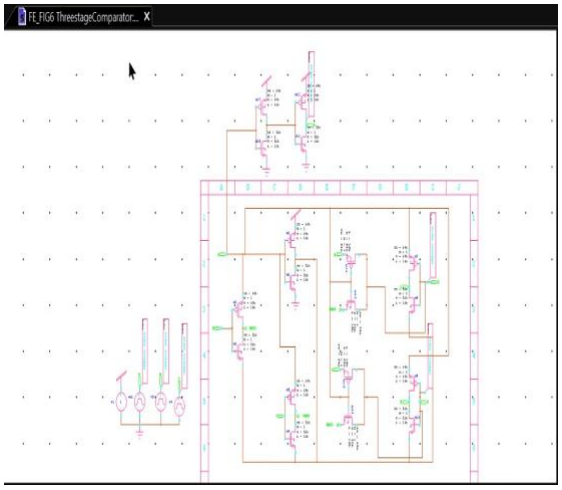


FIG7: Schematic of Modified Fredkin Gate (MFG) in Transistor Level

The above schematic contains the Modified Fredkin Gate (MTG) in Transistor Level. The three inputs are A,B and C. Here the outputs are P,Q and R. The supply voltage used at V1 is 1.8v. For implementing Modified Fredkin Gate (MFG) in Transistor Level 14 transistors are used.

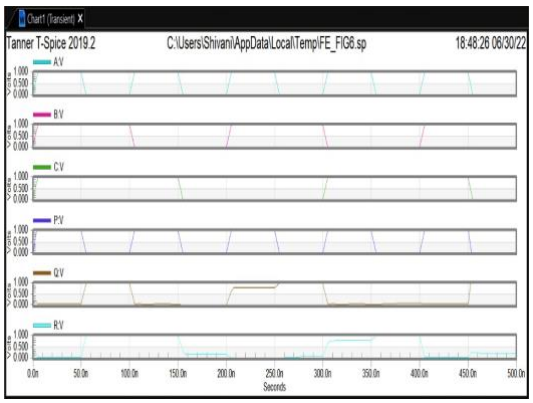


FIG 8: Simulation Output of Modified Fredkin Gate (MFG) in Transistor Level

The accompanying graphic illustrates MFG simulation results on transistor level. Inputs A, B, C, outputs P,Q,R. When A, B, and C are all one, P is one, Q is zero, and R is zero from 0ns to 50ns. When A is zero, B is one, and C is one, P is zero, Q is one, and R is one from 50ns to 100ns. When A is one, B is zero, and C is one, P is one, Q is zero, and R is one for 100ns to 150ns.

When A, B, and C are zero, P, Q, and R are zero from 150ns to 200ns. When A, B, and C are all one, P, Q, and R are all one for 200-250ns. When A is zero, B is one, and C is zero, P is zero, Q is one, and R is zero from 250ns to 300ns. When A is one, B is zero, and C is one, P is one, Q is zero, and R is one from 300ns to 350ns. When A, B, and C are all zero, P, Q, and R are all zero for 350 to 400 ns.

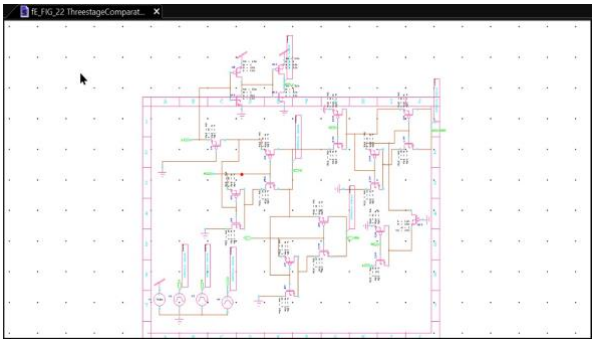


FIG 9: Schematic of Reversible Full Adder using TSG

Above is a TSG Reversible Full Adder. A,B, Cin are inputs. P, Q, Cout, and Sum are outputs. The supply voltage used at V1 is 1.8v. For implementing Reversible Full Adder using TSG 22 transistors are used.

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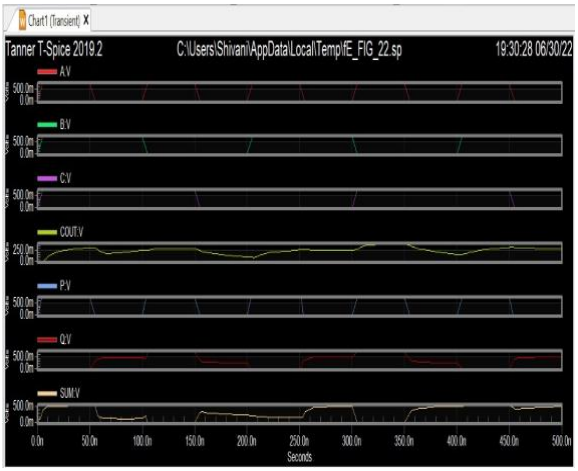


FIG 10: Simulation Output of Reversible Full Adder using TSG

The following diagram exhibits Reversible Full Adder TSG simulation results. A, B, Cin, P, Q, Cout, and Sum are inputs. When logic A, B, and Cin are all one, outputs P, Q, Cout, and Sum are all one from 0ns to 50ns. When A is zero, B is one, and Cin is one, outputs P, Q, Cout, and Sum are zero from 50ns to 100ns. When A is one, B is zero, and Cin is one, P is one, Q is one, Cout is one, and Sum is zero from 100ns to 150ns.

When A, B, and Cin are zero, P, Q, Cout, and Sum are all zero for 150 to 200ns. When logic A, B, and Cin are all one, outputs P, Q, Cout, and Sum are all zero from 200ns to 250ns. When A, B, and Cin are zero, P is zero, Q is one, Cout is one, and Sum is one from 250ns to 300ns. When A is one, B is zero, and Cin is one, P, Q, Cout, and Sum are all one from 300ns to 350ns. When A, B, and Cin are zero, P, Q, Cout, and sum are all one from 350ns to 400ns.

Power Consumed	Fig 2	Fig 6	Fig 10	Fig 14	Fig 18	Fig 22
Max Power	3.363e-06 at time 2.032e-07	6.049e-05 at time 2.55e-07	7.691e-06 at time 2.875e-09	3.359e-05 at time 3.042e-07	1.778e-06 at time 2.034e-07	2.941e-06 at time 2.524e-07
Min Power	1.269e-08 at time 5.580e-09	1.141e-08 at time 5e-09	9.482e-06 at time 5e-08	3.398e-06 at time 6.25e-10	1.379e-10 at time 2.155e-07	2.281e-09 at time 2.226e-07
Average Power	8.7355-08 watts	1.898e-05 watts	1.762e-05 watts	9.329e-06 watts	5.595e-08 watts	6.161e-07 watts

Table 1: Power consumed at 16nm

III. CONCLUSION

In Reversible logic gates they have low power dissipation, high speed, none of the information is lost and heat dissipation was minimum. In digital electronics major problem was power dissipation. In VLSI, low power dissipation plays a major role. Reversible logic gates are more interested because of low power dissipation.

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