International Journal of Research (IJR)
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Vol. 9 Issue 07
July 2022

Design and validation of ALU using m-GDI at 16nm Technology

Gattu Mounika [1], Janagama Srividhya [2], Janagama Srividhya [3], Guntupalli Midhuna[4], J. Sunil kumar[5]

[1,2,3,4]Research Scholar, Vignan Institute of Management and Technology for Women, Kondapur, Ghatkesar, Medchal -50130.

[5]Assistant Professor, Vignan Institute of Management and Technology for Women, Kondapur, Ghatkesar, Medchal -5013

Abstract

It is suggested to build and develop an 8-bit arithmetic logic unit (ALU) utilising the Gate Diffusion Input (GDI) method. When developing the ALU, the GDI approach leads in reduced power consumption and a decrease in the number of transistors. It reduced chip-area and low power consumption. Here 4T XOR is used in the full adder. In this design 1-to-8 de multiplexer circuit is used . A 8-bit ALU perform 8 different operations .

Keywords— 8 – Bit ALU, MGDI, low power consumption, 16nm technology, 4TXOR , Tanner Tool

I. INTRODUCTION

The Arithmetic Logic Unit (ALU), which is the primary component of a Central Processing Unit (CPU), is responsible for performing all types of arithmetic operations, including addition, subtraction, multiplication, and division, as well as logical operations, including inversion, OR, AND, XOR, multiplexing, and other Boolean operations. An ALU is required for every processing device, whether it is a VLSI chip or application-specific smaller circuits. The power consumption and overall performance of the CPU are markedly enhanced by improving the ALU's architecture.

The majority of VLSI applications, including microprocessors, image and video processing, and digital signal processing, heavily rely on arithmetic operations. The most often used operations include addition, subtraction, multiplication, and multiply and accumulate (MAC). Of course, a major factor that significantly influences the design complexity of bigger circuits is the number of transistors.

The choice of topology, power dissipation, and speed are crucial factors for high speed and low power applications in this submicron CMOS technology area. The use of the Gated Diffusion Input (GDI) technology can solve these problems. The literature reports a number of complete adder design optimization methods. One example of Gate Diffusion Input (GDI) enhanced logic swing and reduced static power dissipation are provided by the lowest power design approach.

Several logic operations may be accomplished using this method with less transistor counts. This approach is appropriate for designing quick, low-power circuits using fewer transistors (as compared to TG and CMOS). On the basis of the GDI approach, many complete adder topologies have been constructed at the circuit level.

The modified GDI primitive cells are built, and their notable differences between CMOS and traditional GDI are contrasted.

Although the GDI technology offers fast speed, low power consumption, and a limited number of transistors, the fabrication process presents the most difficulties. The twin-well CMOS or Silicon on Insulator (SOI) method is required by the GDI approach in order to produce a chip, which raises the complexity and expense of fabrication.

An NMOS and PMOS coupled in parallel form the bidirectional switch known as a transmission gate. It avoids the issue of decreased noise margin and higher static power dissipation, but it necessitates the availability of the control and its complement. The slower speed of this technology and the inability to link more than three transmission gates in a cascade owing to a charge sharing issue are drawbacks.

Pass transistor logic eliminates superfluous transistors, which lowers the number of transistors needed to create various logic gates. Instead of using switches that are linked directly to the voltage supply, PTL designers employ transistors as switches to pass logic levels across the nodes of a circuit. The main drawback of PTL is the reduction in voltage between high and low logic levels at each stage.

In electronic Mathematical operations (such as addition, subtraction, multiplication, and division) are often utilized in a variety of technological applications. A subtractor is a key component in microprocessor tasks such as image processing and digital signal processing.

The basic component needed to subtract two binary digits is a one-bit subtractor. One NOT gate, one XOR gate, and one AND gate make up this structure. A complete subtractor is a combinational circuit that conducts subtraction using three bits: the borrow from the previous stage, the minuend bit, and the subtract end bit. It generates two outputs, difference (D), and borrow out (B). As more logic gates are needed to create a complete subtractor, more transistors are needed, which requires more space on the device.

Consequently, duration, energy usage, and area Due to the increased usage of portable IC devices like MP3 players, mobile phones, and PDAs, among others, IC engineers are needed to enhance the performance of current operating modules, particularly in terms of size and power consumption. IC designers have faced greater limitations due to the fact that battery technology is not developing as quickly as microelectronics technology. These limits include fast speed, high throughput, tiny silicon area, and low power dissipation.

II. PROPOSED SYSTEM:

The use of the gate diffusion input approach allows for the reduction of digital circuit size, propagation delay, and power consumption while retaining a low level of complexity in the logic architecture. In GDI technique consists of 4terminal s G, P, D, N. Where G acts as common gate for pmos and nmos. P terminal acts as source/drain for P-channel . Similarly n terminal acts for N-channel.

International Journal of Research (IJR)
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Vol. 9 Issue 07
July 2022

This three terminals acts as input terminals. Where D acts as output for collector. In this paper demux and mux plays vital role. 1:8demux acts as input for implementing logic and arithmetic operations such as full adder, Nand, Xor, buffer are etc. Vo acts as input for 1:8demux where so, s1, s2 are selection lines and Y1, Y2.. Y8 are outputs of demux. This selections lines and outputs acts as input for mux. According to Y values we can connect 2:1 mux for each Y value and then will be connect half adder, full adder, full subtractor, Nand, NOR, Comparator and And.

In this paper we can observe less power, delay and Number of transistors count reduces. Tanner EDA tool version 13.0 has been utilized throughout the whole study project for simulation purposes.

III. BLOCK DIAGRAM

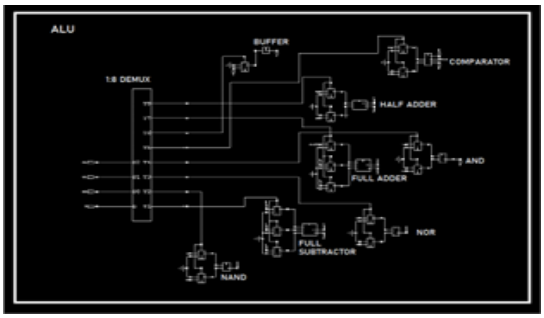


Fig : Block Diagram of 8 – Bit ALU

COMPONENTS

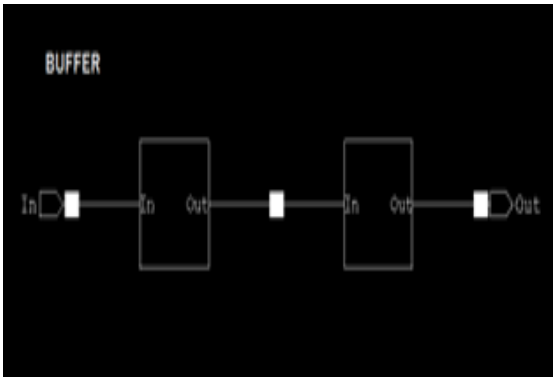


Fig : Buffer

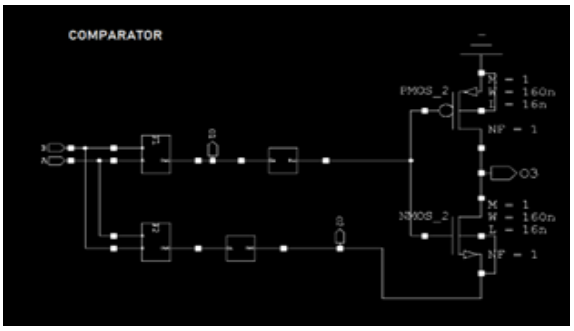


Fig :Comparator

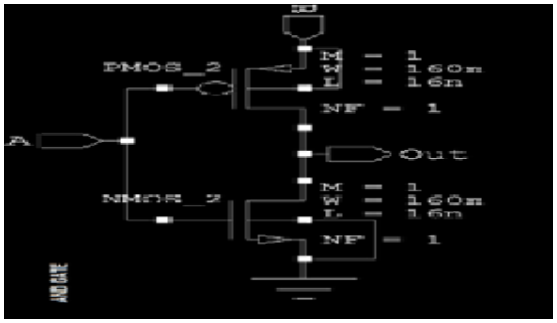


Fig: AND

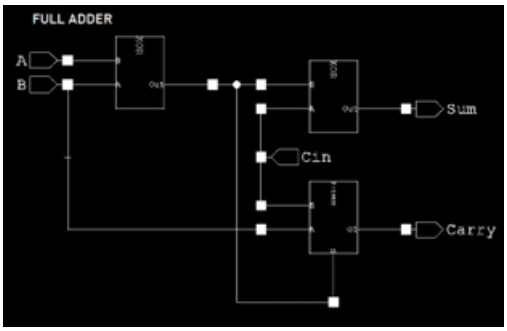
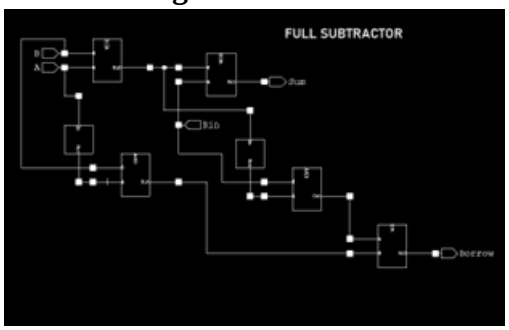


Fig : Full Adder



International Journal of Research (IJR)
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Vol. 9 Issue 07
July 2022

Fig: Full Subtractor

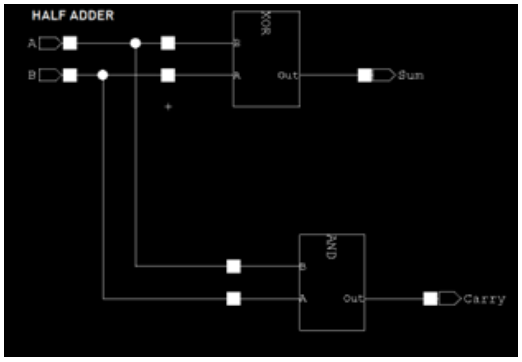


Fig: Half Adder

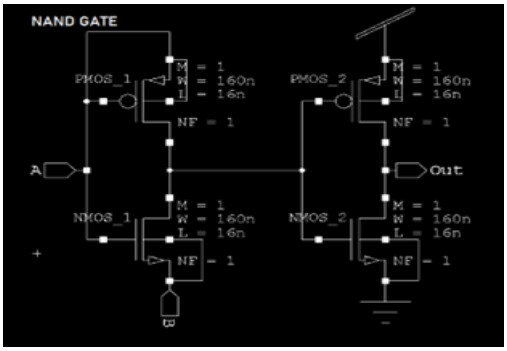


Fig: NAND

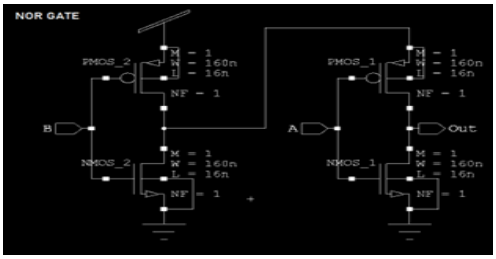


Fig :NOR

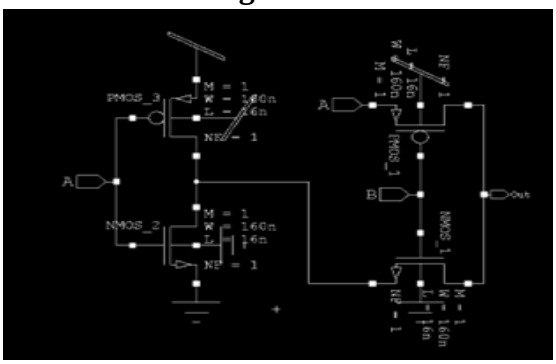


Fig : 4TXOR

IV. RESULTS & DISCUSSIONS

WAVE FORMS :

Full Subtractor

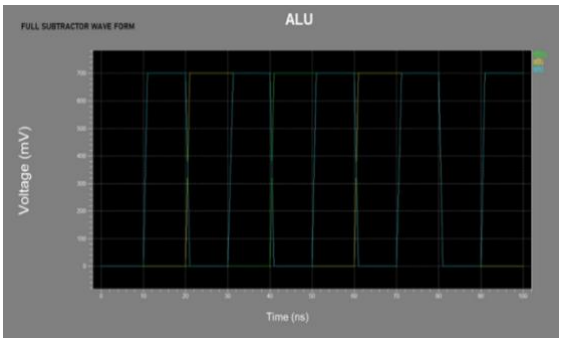


FIG : FULL SUBTRACTOR WAVE FORM

NAND

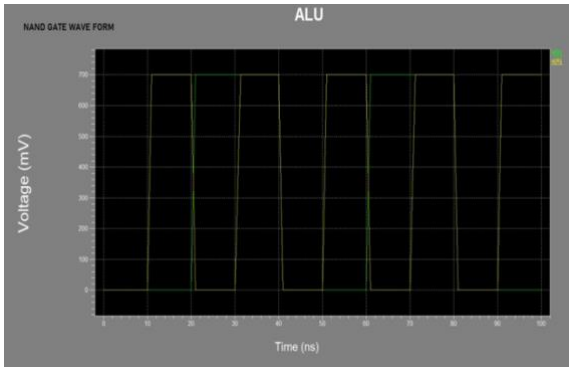


FIG: NAND GATE WAVE FORM

NOR

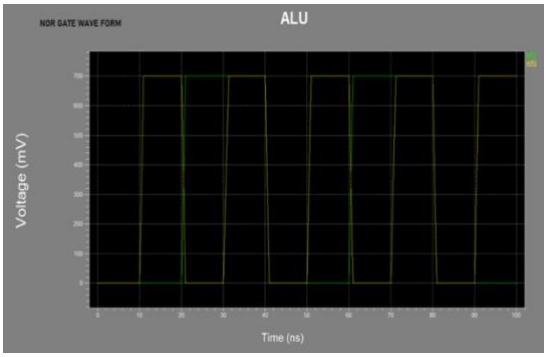
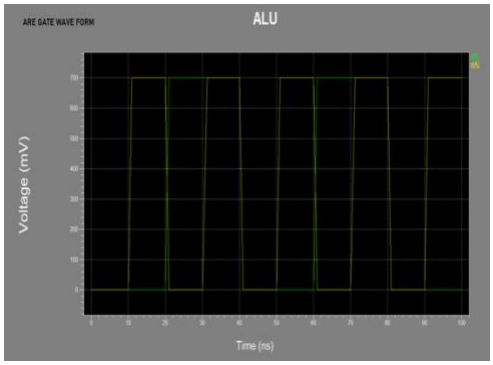


FIG : NOR GATE WAVE FORM

AND



International Journal of Research (IJR)
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Vol. 9 Issue 07
July 2022

FIG : AND GATE WAVE FORM

COMPARATOR

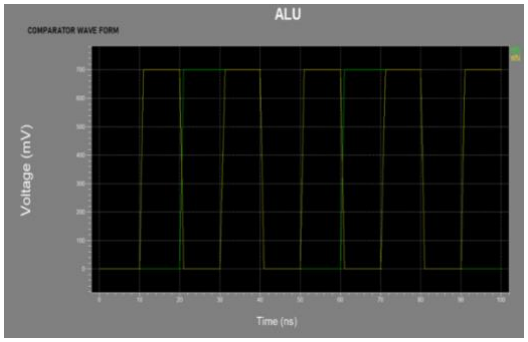


FIG : COMPARATOR WAVE FORM

BUFFER

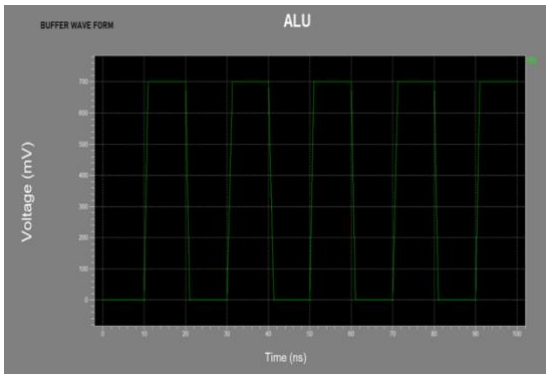


FIG : BUFFER WAVE FORM

FULL ADDER

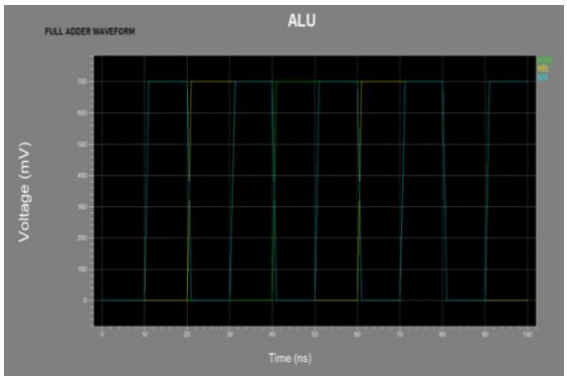


FIG : FULL ADDER WAVE FORM

HALF ADDER

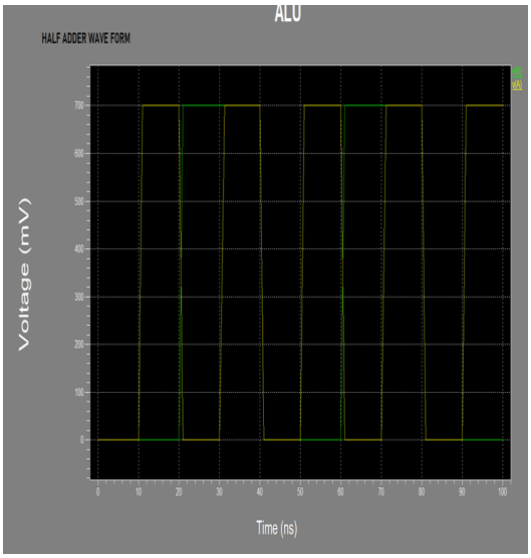


FIG: HALF ADDER WAVEFORM

OUTPUT WAVE FORM OF 8-BIT ALU

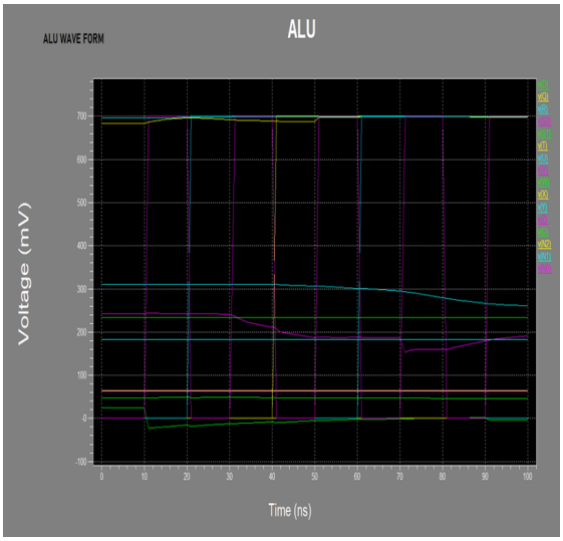
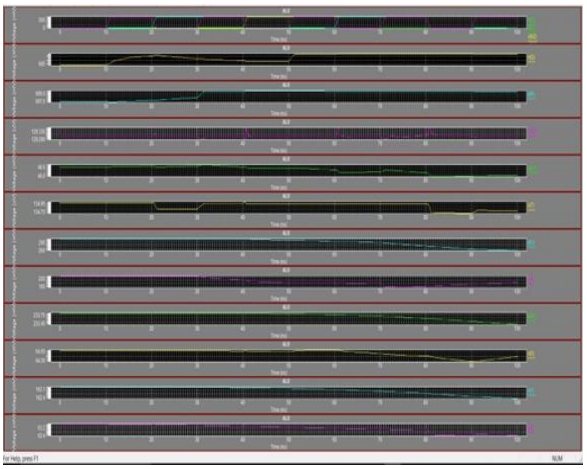


FIG : output of 8 – bit ALU Wave form

IV. RESULT



Simulation results for Proposed 8-Bit ALU

DESIGN	Number of Transistors	Delay	Power
8-Bit ALU	120	5.8775e-008	Avg power: 9.353481e-006 watts Min power: 5.720211e-006 at time 9e-008 Max power: 1.233122e-005 at time 1e-009

TABLE: 8 – BIT ALU VAUE

V. CONCLUSION

The suggested 8-bit ALU uses fewer transistors, uses less power, and has less delay. In this, a new 1:8 demultiplexer circuit was designed and a 4T XOR full adder was employed.

References

[1] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low- power CMOS digital design," IEEE J. Solid-State Circuits, vol. 27, pp. 473–484, Apr. 1992.

[2] A. P. Chandrakasan and R.W. Brodersen, "Minimizing power consumption in digital CMOS circuits," Proc. IEEE, vol. 83, pp. 498–523, Apr. 1995.

[3] Arkadiy Morgenshtein, Alexander Fish and Israel A. Wagner, "Gate-Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits", Ieee Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 10, No. 5, October 2002.

[4] L. Bisdounis, D. Gouvetas and O. Koufopavlou, "A comparative study of CMOS circuit design styles for low power high-speed VLSI circuits" Int. J. of Electronics, Vol.84, No.6, pp 599-613,1998.

[5] N. Weste and K. Eshraghian, Principles of CMOS digital design. Reading, MA: Addison- Wesley, pp. 304–307.

[6] Oh-Hyeong Kwon, "A Boolean Extraction Technique for MultipleLevel Logic Optimization" IEEE 2003.

[7] R. Uma, "4-Bit Fast Adder Design: Topology and Layout with Self- Resetting Logic for Low Power VLSI Circuits" International Journal of Advanced Engineering Sciences and Technology, Vol No. 7, Issue No. 2, 197 205, 2011.

[8] R. Uma and P. Dhavachelvan "Analysis on Impact of Behavioral Modeling in Performance of Synthesis Process The second International Conference on Advances in Computing and Information Technology, July 2012, Published in Advances in Intelligent Systems and Computing book series of Springer, Pg593-602.

[9] R. Uma and P. Dhavachelvan, "Modified Gate Diffusion Input Technique: A New Techniqu for Enhancing Performance in Full Adder Circuits", Procedia Technology 6 (2012) 74 – 81.

[10] R.Uma, Vidya Vijayan, M. Mohanapriya, Sharon Paul, "Area, Delay and Power Comparison of Adder Topologies", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012

[11] S. Sweta and Md. Afreen Begum, "Design of High Speed, Area Optimized and Low Power Arithmetic and Logic Unit", Advances in Industrial Engineering and Management,Vol.6, No. 1 (2017), 26-31.

[12] Shubham Sarkar, Sujan Sarkar, Tarunesh Pati, Indranil Monda, Asif Iqbal, Joy Sengupta, Alojyoti Mistry, "Low Power implementation of Multi-Bit Hybrid Adder using Modified GDI Technique", 2018 International Conference on Electronics, Materials Engineering & Nano-Technology.