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Real-Time Self Repairable Multiplexer for Fault Tolerant Systems

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Abstract

More transistors may be put on a single chip when using VLSI. The system or chip is increasingly prone to errors when the distance between transistors or circuits decreases. Inaccurate outcomes must be prevented via fault tolerant systems. A device called a multiplexer chooses input signals depending on a choose signal. The sole self-checking multiplexer is the subject of the current works.

A self-repairing 2:1 multiplexer that can fix both permanent and temporary errors is suggested in this research. The self-repairing multiplexer is offered with two distinct designs. The first design includes extra circuitry to fix the multiplexer problem. The OR and AND gates that make up a multiplexer are self-repairable in the second design. The single and multiple defects may be detected and fixed by these self-repairing multiplexer designs. The suggested architectural designs provide 100% error recovery. With the help of the Cadence tool, the functioning of the circuits is checked.

Index Terms— VLSI, Fault, Error, Self-checking, Self-repairing.

I. INTRODUCTION

A circuit's answer might be invalid due to the existence of faults. This yields unreliable outcomes. To endure errors, systems that are fault-secure are very necessary. Therefore, self-checking and self-repairing are essential for the circuit to operate properly. In self-checking, the circuit itself finds the issue, and in self-repairing, the circuit may fix itself and provide the desired output. Individual circuit gates affect how well a circuit performs overall. Designing with fewer gates may improve performance in terms of delay, area, and power.

The critical route should be as short as feasible to achieve high speed. Similar to this, fewer gates are employed at the circuit level to achieve low power without sacrificing the circuit's precision. A broad range of applications, including adders, multipliers, communication, digital signal processing, etc., employ multiplexers.

The input data will be chosen by the multiplexer and sent to the output based on the selection signal. Incorrect data is produced when a multiplexer is malfunctioning. In order for the multiplexer to produce accurate data even with faults, it must be fault secure.

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II. EXISTING SYSTEM

In existing model the full adder which consists of AND, OR gates and 2X1 MUX are designed with the 65nm technology. In existing method the factors in terms of power, delay, power delay product are optimized in high speed and average power consumed is very high and power delay product is more, the noise margin is high and other factors like drive capability are more so in order to resolve this issues we are going to proposed model with 45nm technology.

This simulation of AND Gate with and without faulty occurrence. In multiplexer there may be fault This may lead to improper results, so fault free architecture is very useful to suspect the faults. The performance of the system depends upon the gates used in the design of circuit. The performance of proposed design can increase in terms of power PDP and delay by using limited gates.

The simulation of OR Gate with and without fault a logic operation which gives the value one if at least one operand has the value one, and otherwise gives a value of zero this is an without fault in with fault inverse of OR Gate.

III. PROPOSED SYSTEM

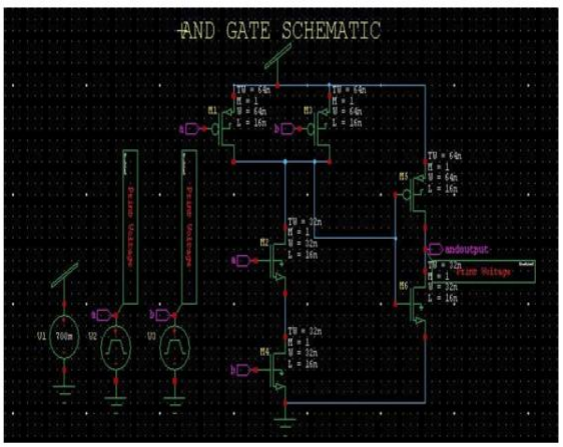

Fig 1. Schematic of AND gate without fault

The above figure represents the schematic of AND gate which is combinations of number of PMOS and NMOS logic is designed in 65nm technology. It is designed with tanner S-EDIT Tool.

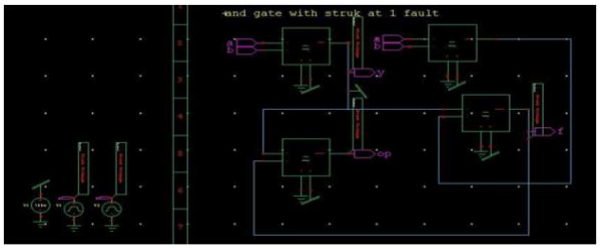

Fig 2. Schematic of AND gate with fault

The schematic for a defective AND gate, which combines a number of PMOS and NMOS logic elements, is shown in the above picture. It was created using 65nm technology. It was created using the S-EDIT Tool.

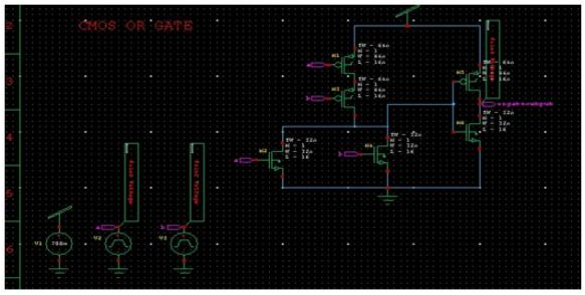

Fig 3. Schematic of OR gate without fault

The simulation results of an OR gate without a problem are shown in the above image. CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool is used to simulate it. W-EDIT is used to analyse wave shapes (wave form editor).

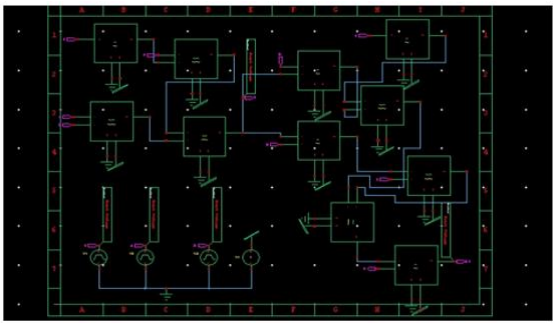

Fig 4.Schematic of OR gate with fault

The above figure shows the schematic of faulty OR gate which is combinations of number of PMOS and NMOS logic is designed in 65nm technology. It is designed with tanner S-EDIT fig 5. 2x1 multiplexer without fault.

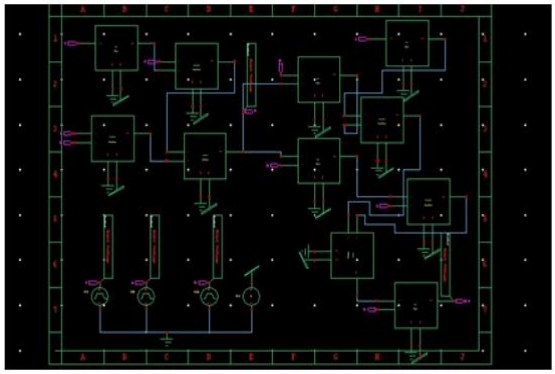

Fig 5. Schematic Of 2X1 MUX without fault

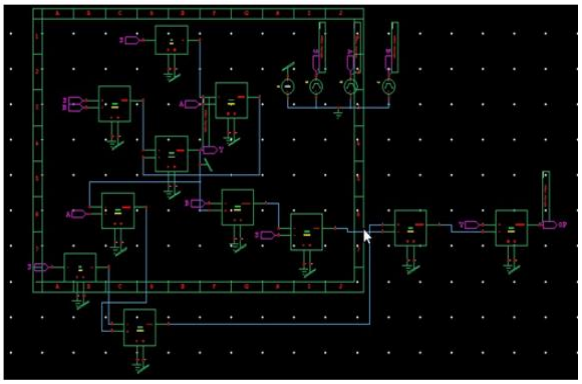

Fig 6. Schematic Of 2X1 MUX with fault

The above figure shows the schematic of faulty 2X1 MUX which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool.

IV. RESULTS

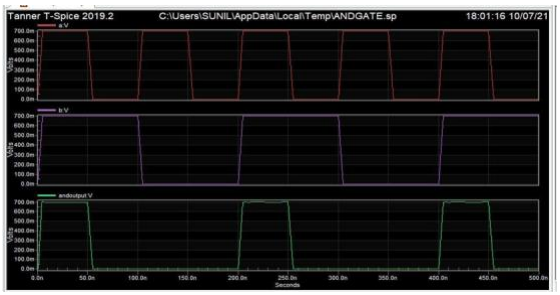

Fig 7. Simulation of AND gate without fault

The graphic above displays the outcomes of a simulation of an AND gate. It is simulated using the CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Wave shape analysis using W-EDIT (wave form editor).

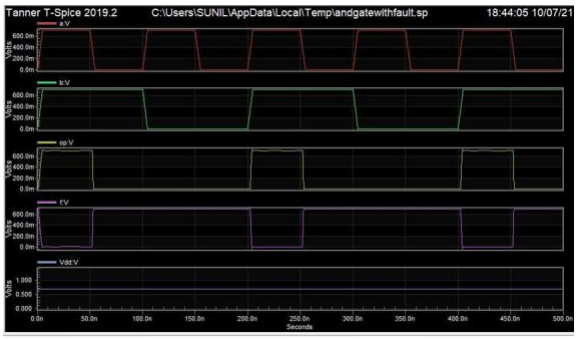

Fig8.Simulation of AND gate with fault

The fault AND gate simulation results are shown in the above figure. CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool is used to simulate it. W-EDIT is used to analyse wave shapes (wave form editor).

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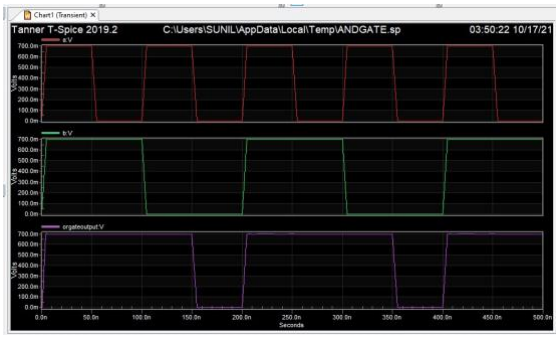

Fig 9. Simulation of OR gate without fault

The simulation results of an OR gate without a problem are shown in the above image. CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool is used to simulate it. W-EDIT (wave form editor) is used to examine wave forms).

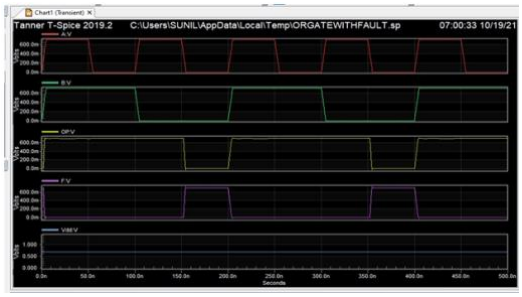

Fig 10. Simulation of Faulty OR Gate

The fault OR gate simulation results are shown in the above figure. CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool is used to simulate it. W-EDIT is used to analyse wave shapes (wave form editor).

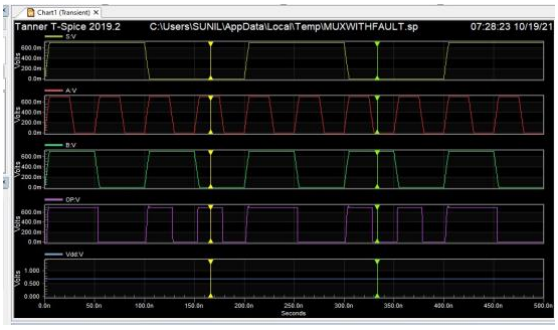

Fig 11. Simulation Of Faulty 2X1 Mux

The simulation results of a flawed 2x1 mux are shown in the above graphic. CMOS Tanner's SPICE (Simulation Program with Integrated Circuit Emphasis) Tool is used to model it. W-EDIT (wave form editor) is used to examine wave forms).

V. CONCLUSION

Since the multiplexer plays a crucial role in many systems, malfunctions in the multiplexer cause the systems' findings to be erroneous. To prevent failures, fault tolerant systems must include a fault tolerant multiplexer. The self-repairing multiplexers that are being suggested may be employed in multipliers, multi-bit adders, etc. To achieve 100% error recoverability, the suggested self-repairing multiplexers may be used in fault tolerant systems. Without the need for outside assistance, the structure can restore itself. This stays away from the space above. The outputs of the circuits are checked by simulation. The suggested structures' fault tolerance is confirmed.

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