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Design and Analysis of Three-Stage Comparator and Its Modified Version with Fast Speed and Low Kickback

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Abstract

This paper proposed a CMOS Three modelled comparator and its new version to enhance the speed and reduce the noise. When validate with conventional comparators this proposed comparator will enhance additional amplification structure, with this the efficiency of the proposed model will increase enormously. With this the proposed model the speed of the comparator will increases because inputs are driven with input pairs for regeneration and amplified stage. With this structure speed increased a lot. By this proposed model noise generated by the Pmos topology will dwindles by the use of Nmos pair. In proposed model an extra signal has been configured in the regeneration stage, in turn will enhance the speed of the proposed circuit will increase further. To validate the proposed model, using 16nm BSIM4 Model. By comparison, proposed model dictates that three stage circuits enhance speed by 34% and dwindles noise by several times. The proposed model has been validated through Mentor graphics 16nm BSIM4 Technology.

I. Introduction

Several types of ADCs rely on comparators [1, 2]. The sampling rate and precision of high-speed, high-resolution SAR ADCs are limited by factors such as the speed of the comparator, the magnitude of kickback noise, the level of input referred noise, and the magnitude of the offset. Creating a high-performance comparator is crucial.

Strong ARM architecture provides so many advantages due to positive feedback nature provides low static power consumption, and provides highest comparison with low leakage currents. But it has some limitations. The primitive problem raised with source current in latch, due to this leakage current the speed of the comparators is limited. This leakage current is constructed by the pair of the input stage of the Strong ARM.

Due to the common mode stage across the input stage current is limited with half of the bias voltage. Due to more number of transistors for the configuration, consumes more power supply voltage is needed. In Two stage model of comparator, less effected by the source leakage current.

This is a Miyahara's Two stage architecture. This architecture regeneration speed never controlled by the source current because of its input mode transistors i.e. M6-M7 is biased by the supply voltage of VDD/2; this biased voltage is almost double when it is compared to Strong ARM latch. For the two-stage design consumes less number of

transistors hence the requirement of supply voltage dwindles more.

Even though two stage structures possess higher speed, that speed can be increases further by changing the topology.

The change in configuration of transistors i.e PMOS transistors with NMOS Transistors, by change with this transistors performance increases further, this configuration paly an essential component at the pre amplifier stage. Traditionally replacement of NMOS transistors will increases speed further, when compared with PMOS transistors.

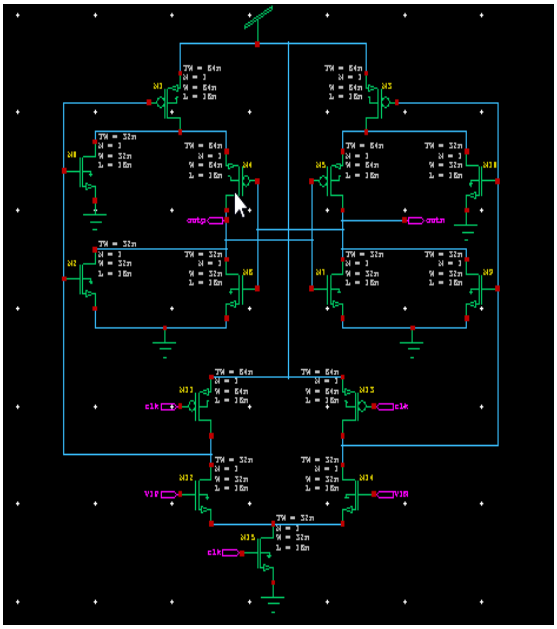

Fig 1: miyaharas two stage comparator

Figure 1 shows Miyahara's 2-stage comparator. Reset, amplification, and regeneration. CLK resets comparator (reset phase). During the amplification phase (CLK = 1), VIP-VIN is sent to the latch. Outputs regenerate to VDD or GND.As previously established, the latch stage of such a device is restricted to pMOS input pairs.

Miyahara's two-stage comparator is faster, but it can be better. The latch input pair M6-7 are pMOS transistors, and their poor hole mobility (2-3 times lower than nMOS electron mobility) slows regeneration. To speed up regeneration, we'll replace the latch input pair with nMOS transistors. Preamplifier input pair nMOS transistors must be maintained.

II. THREE-STAGE COMPARATOR

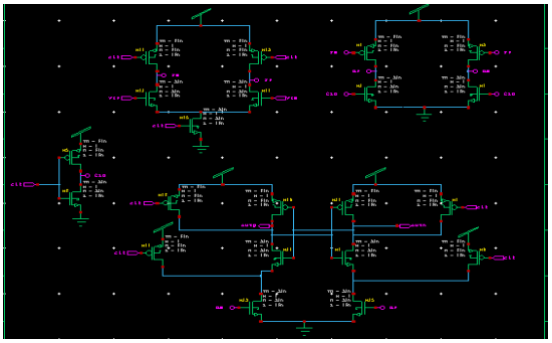

Fig 2: three stage comparator with preamplifiers and latch stage

Figure 2 depicts the three-stage comparator utilised in this investigation. Each of the three phases builds on the previous one. The second stage preamplifier is the main difference between this comparator and Miyahara's comparator. This additional preamplifier functions as an inverter, allowing the latch stage to utilise nMOS input pair M11-12 instead of pMOS, resulting in quicker performance. The additional preamplifier boosts regeneration efficiency and reduces offset and noise.

However, the time it takes for the amplified signal to reach the latch stage rises when a preamplifier is also included. So, it's important to figure out if the extra delay is worth the value it adds. Fig. 2 shows that after the initial amplification, FP and FN are connected to GND. This creates a VDD-level gate-source voltage for M8-9. M8-strong 9's current quickly pulls up RP and RN. Second stage post-layout simulation latency is 20 ps shorter

than latch stage (about 200 ps in post-layout simulation).

The second stage is a low-delay dynamic inverter, so this makes sense. Compared to Miyahara, Fig. 2's first-stage comparator output load is only M8-9. (Fig. 1, M6-7, M12-15). Reduced load speeds amplification.

When compared with the existing topology [13], the proposed architecture contains one extra module that is pre amplifier stage also called as the second stage is added. All the stages are configured as one after the other. This added extra pre amplifier stage act as a inverter by transistors M11-12 Instead of PMOS transistors pairs[14].by this added configuration enhances speed of the comparator circuit.

Before going to the last stage, signal has to propagate through two stages, due to propagation through different stage leads to decreases the speed of the comparator, even though strong in providing higher voltage gain, with reduced noise. The delays are occurred due to connecting the nodes FP and FN to GND. This nodes are connected to the transistors M8-M9 have produce large gate to source voltage drop.

III.PROPOSED MODIFIED VERSION OF THREE-STAGE COMPARATOR

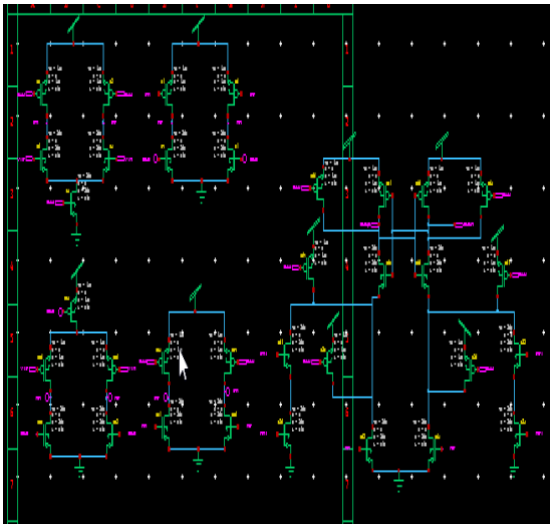

Fig. 3. Schematic of Modified three-stage comparator. (a) Preamplifiers with nMOS input pair. (b) Preamplifiers with pMOS input pair. (c) Latch stage

To enhance the comparator speed, to reduce kickback noise here we introducing new architecture that is modified model with three stage comparator. As shown in Figure 3, when it compared to the traditional comparator circuit, basically modified comparator model contains, Figure 3. (b) Design with two stage comparator and Figure 3.(c) designed with latch stage with the help of M29-32 transistors. PMOS transistors are used to design first stage.

The operation of three stage modified model is as follows. in the reset stage , when clock equals to zero, and clock bar equal to one , the nodes RP1 and RN1(where R for Rise) in Figure 3 (b) are shorted to Ground terminals and rest of the nodes FP1 and FN1(Where F for Fall) are shorted to VDD. Due to this configuration of biasing transistors M30 and M32 are in cut off mode in Figure 3(c). Due to these arrangements there is no chance of flowing

static current flow in the transistors M29-M32.

Next stage of operation is amplification stage, in this stage CLK is raised to logic 1 and CLKB is falls to logic 0. Where RP1 and RN1 in Figure 3(c) raises to VDD. Then Nodes FP1 and FN1 are drops to logic 0.this happen due to rising of RP1 and RN1 before falling of FP1 and FN1.from the nodes of OUTP and OUTN there is a differential current produces by the latching connections, this is due to an extra path in Figure 3(c).

The resulting differential voltage at OUTP and OUTN is utilised to reduce noise and accelerate regeneration while reducing noise. When FP1 and FN1 are set to logic 0, the additional route in Figure 3 (c) is switched off, which helps to increase speed while decreasing static current.

The revised three-stage comparator improves speed, reduces input referee offset and noise, and reduces kickback noise. It is a high-speed and high-resolution SAR ADC. The updated version may be used with the SAR ADC that uses time-interleaved noise shaping described in [13]. Limitations in ADC resolution and sampling rate are a result of kickback noise and the speed of the comparator [13].

Zhuang et al. [13] split channels in order to reduce kickback noise, however doing so adds complexity to the system. These difficulties can be addressed with the improved three-stage comparator. It is the quickest and most silent comparer.

B. Design Consideration:

Integration time and input pair trans conductance inversely affect comparator input noise. High-speed ADCs shorten comparator integration time. Increase input pair trans conductance to reduce input referred noise (includes the input pair of each preamplifier as well as the latch stage).This study employs huge input pair sizes (W/L = 3 m/0.13 m).

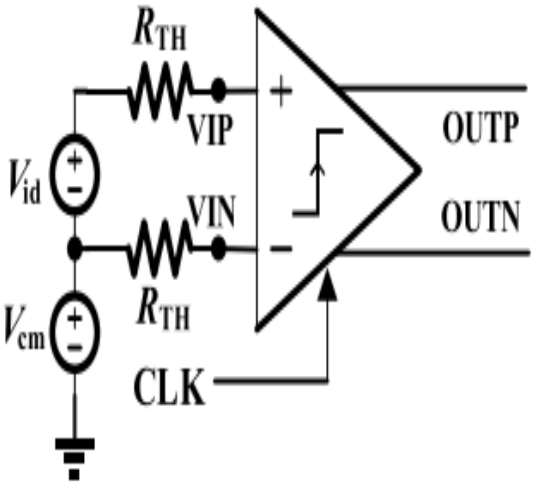

Fig 4:Circuit for evaluating kickback

IV. SIMULATED AND MEASURED RESULTS

TABLE I:COMPARISON WITH STATE-OF-THE-ART WORKS

	Comparison of three stage comparator and its modified version with fastest speed and low kickback					
	Miyahara Two- stage comparator		Existing three stage comparator		Proposed three stage comparator	
Technology	65nm	16nm	65nm	16nm	65nm	16nm
Supply voltage	1.8	0.7	1.8	0.7	1.8	0.7
MOSFETs	15	15	19	19	32	32
Delay(ns)	99.96	53.43	399.75	0.77	249.64	25.01
Power (uw)	31.247	0.0801	6.55	150.166	227.03	0.38

Table 1. Comparison of CMOS three stage comparators

The three-stage comparator and its modified variation are the ones with the shortest delays.as can be observed. The slightest kickback noise is also present in the updated version. Despite the increasing circuit complexity, the size and power consumption are also less.

V. CONCLUSION

This short shows the three-stage comparator and a modified version of it. Both are fast, make little kickback noise, and have little offset and noise that come from the input. These comparators work best with the high-speed, high-resolution SAR ADCs. Lastly, results that can be measured show that these comparators work.

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