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Design and Simulation of Multistage Hybrid full adder using CMOS 16nm Technology

S. Sukeerthi[1], N. Sirisha[2], P. Varshitha[3], S. Sindhu[4], J. Sunil Kumar [5]

[1,2,3,4] Research Scholar, Vignan Institute of Management and Technology for Women, Kondapur, Ghatkesar, Medchal -50130.

[5]Assistant Professor, Vignan Institute of Management and Technology for Women, Kondapur, Ghatkesar, Medchal -50130.

ABSTRACT

The assessment of the timing behavior of the arithmetic circuits is one of the most challenging aspects of the design of extremely large scale integrated circuits. The concept of logical effort provides a helpful framework for analyzing and assessing the timing behavior of typical CMOS (C-CMOS) built circuits. This approach does not work well for hybrid circuits. However, various hybrid circuits that are faster than C-CMOS ones and utilize less power than C-CMOS ones have been proposed for usage in a wide range of devices, including portable and Internet of Things devices. In this respect, it is unavoidable that a straightforward and effective timing behavior approach, such as traditional logical effort, be present and used for the study of hybrid adder circuits. This paper presents an effective analysis and modeling approach to help designers evaluate the timing behavior of hybrid full adder circuits at the block level and anticipate their performance in multistage circuits. For precise selection and optimization of the hybrid adder cells that can be seen on a single test bench, the gain and selection factor is recommended in order to optimize the trade-off between energy efficiency and performance. Utilizing 16-nm CMOS technology, the suggested technique is examined.

I. INTRODUCTION

FULL adders are the essential mathematical component of all computer systems [1], from the simplest controllers to the most sophisticated processors. The complete adder has been a focus of attention for arithmetic blocks in recent years, particularly for various applications including mobile and IoT [2], [3]. There are several logic designs that may be used to create complete adders, and each logic design has benefits and drawbacks.

Pull-up and pull-down transistor metal-oxide semiconductor (C-CMOS) the most preferred logic type for creating extremely large-scale integrated circuits. Pull-up networks are composed of series and parallel pMOS transistors, and pull-down networks are composed of parallel nMOS transistors. The usual CMOS construction is a C-CMOS type full adder with classic pull-up and pull-down networks that provide it with powerful driving capabilities and full output swing.

On the contrary. C-CMOS circuits use more power than hybrid logic circuits because of the increased short circuit current and the changing current during switching time. In general, hybrid structure circuits contain fewer power and ground connections than C-CMOS circuits. In addition, the number of connections

between the pMOS and nMOS transistors in a C-CMOS complete adder increases the capacitance at the input, which in turn slows the adder's performance.

The goal of the hybrid logic style is to improve the design's performance by combining the advantages of several logic approaches during implementation [3, 6]. The majority of the circuits described in the hybrid structure are full adders, which is significant since the circuit becomes much more complex as the block size and number of inputs and outputs, such as compressors, carry save adders, etc., rise.

II. LITERATURE REVIEW

Examining the capabilities of complete adders at 0.18 nm in tree-based arithmetic circuits, In order to carry out specialized algorithms like convolution, correlation, and digital filtering, For digital signal processors and application-specific integrated circuits to function properly, arithmetic circuits are essential. The majority of the time, the maximum performance of integrated circuits is constrained by the optimal method for including arithmetic operators in the cell library provided to the designer for synthesis.

As the number of transistors on a chip and its clock speed continue to expand in tandem with the complexity of arithmetic circuits, the need to minimize power consumption is more pressing than ever. To facilitate the creation of cell libraries, many CMOS logic types have emerged. They will most likely ensure that integrated circuits may continue to advance in performance while simultaneously decreasing the cost-per-function.

Since ultra deep submicron technology has made threshold voltages much lower, the most obvious way to cut down on power use is to lower the supply voltage. But lowering the supply voltage slows down the circuit and makes it harder for cells built with certain logic designs to be driven. Clustered voltage scaling (CVS) and dual voltage supply (dual-VS) are two new proposals [1, 2] for maintaining chip throughput stability.

In order for these solutions to be effective, the performance of the fundamental cells that dominate the critical route must be determined in the desired technology and application environment over a variety of supply voltages. Addition, multiplication, division, exponentiation, and other complicated arithmetic circuits all rely on a full adder [3–6]. There are two primary functions for complete adders in computational mathematics.

Chain organized applications like ripple carry adders (RCA) and array multipliers fall within one group [7], [8]. In such contexts, the complete adders' carry-in and carry-out nodes often lie along the crucial route. Quick signal generation for the carry-out is required. Otherwise, the worst-case delay would be prolonged, and there will be more glitches in the latter stages, resulting in increased power dissipation due to the slower carry-out generation.

III. THE PROPOSED DESIGN

The timing analysis techniques used in industry might also benefit from the research presented in this study. In this work, we try to answer the question, "What are the most important factors a designer must consider for hybrid circuits

on a single test bench in order to get the whole timing behavior of the adder cells?" The timing behavior of hybrid full adders with an odd design is investigated in a novel manner in an effort to simplify matters.

The most common hybrid full adders are the transistor function full adder (TFA), the transmission gate full adder (TGA), the New-HPSC, and the New-14T [10]. (Fig. 1). These full adders are perfect for running this new method because they have different input-output drive conditions than C-CMOS full adders.

Propagation delay may not be a good way to describe how the cell's timing works because it depends on the test bench and its properties depend on how the input and output are driven. The proposed method considers three factors for determining the behavior of full adders over time. This includes switching speed, driving capabilities, and input capacitance.

By analyzing some of these characteristics on a single test bench [Fig. 2(c)], a designer may forecast how a multistage adder cell will function as a whole. As test benches for the multistage analysis of carry and sum output signals, the ripple carry adder (RCA) and the 6:2 compressors are used. Since the RCA has a route drive with many stages, it is a good way to figure out how the carry signal's timing works (see Fig. 3(b)).

They've decided to use a 6:2 compressor, which they'll cascade in a five-stage arrangement [Fig. 3(a)], so that we can extract the temporal behavior of the cumulative signal. This analysis is done for all chosen complete adders. First, the complete adders have been appropriately scaled to optimize the power delay product (PDP) utilizing the SEA [10] as a powerful technique for studying timing behavior. When typical MOSFETs are shrunk to dimensions below 20 nm, electrical properties begin to decline.

Fin FET technology is chosen to replace Bulk CMOS because it enables transistors to be reduced down even further while offering promised improvements over Bulk CMOS, such as higher drain current, lower switching voltage, and much lower static leakage current [14]. Due to its superior capacity to generate greater current at reduced size and lower input voltages, FinFETs have shown superior performance in comparison to Bulk CMOS in terms of speed and power.

In this research, we also address the subject of how the aforementioned timing analysis approach with its three parameters performs across various technologies. Therefore, both Bulk CMOS full adders and Fin FET full adders are analyzed and contrasted in terms of their timing capabilities. In this work, 32-nm Bulk CMOS and shorted gate Fin FET models are used for all HSPICE simulations.

Variation in Driving Capability and Switching Time

MULTISTAGE ANALYSIS

Using the 6-to-2 compressor [Fig. 3(a)] and the 4-bit RCA [Fig. 3(b)], the multistage analysis is performed. The carry signal is a crucial component of the overall signal in both a 6:2 compressor and a 4-bit RCA. To have a better understanding of how the timing of the cells changes as there are more stages, the transition time for all input pulses has been fixed.

The load on each output stage's capacitor has been changed from 0 to 2 fF, and all input pulses go through the input buffer. The unit inverter has been utilized for Cin and other single test bench measurements. Buffers of sizes W/L 5/3 and 12/5 [10] have been utilized for multistage analyses that need increased drivability at the first stage; as a result, the delay associated with the first stage now includes the delay introduced by the buffer.

Figures displays the total and carry outputs from the simulation for the entire adders. Figure 4 demonstrates that the output delay lines of C-CMOS and New HPSC full adders have identical slopes. The output inverters are responsible for this consistent slop, which makes the vehicle simple to drive. Because and T Do are the same for all stages, the length of each line from stage 2 to stage 4 is same.

This means that no matter how many stages there are, we can expect the same behavior. Compressor research on TGA and TFA full adders demonstrates that each of the four phases displays distinct behavior, with a constant TDo and a known range. TGA complete adder RCA shows predictable stage-to-stage change in and constant TDo.

In the TFA full adder's RCA analysis, it is anticipated that both and TDo would fluctuate from stage to stage. It is possible to foresee the behavior of C-CMOS, New-HPSC, TFA, and TGA full adders with arbitrary stage counts. The 14T full adder performs horribly and produces incorrect results in compressor analysis because of its weak drive and excessive input capacitance. Observing the RCA of the New-14T full adder reveals unpredictability in the values of and TDo over the many stages.

Connecting an output buffer allows for accurate prediction of the New14T full adder's behavior, but does add some space and power requirements to the cell. Table III explains why slope and TDo may change from stage to stage for each of the complete adders we've discussed. As can be shown in Table III, there is no difference between C-CMOS and New-HPSC in terms of drivability or inherent latency.

IV. RESULTS

On this work, we focus on answering the question, "What are the most significant considerations for the designer of a hybrid structure circuit in a single test bench? For obtaining the whole behavior of the time of adder cells?" In light of this, a novel method is presented for assessing the timing behavior of hybrid full adders with an unconventional design, based on the principle that things should be as straightforward as feasible.

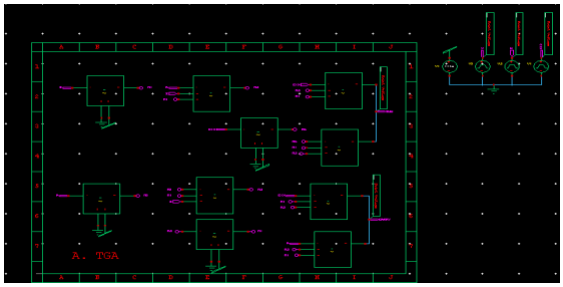

Fig1: Adder with full-transistor functionality (TFA)

The most common hybrid full adders are the transistor function full adder (TFA), the transmission gate full adder (TGA), the New-HPSC, and the New-14T [10]. (Fig.1). These full adders are controlled differently than the C-CMOS full adder that is necessary for this new way to function.

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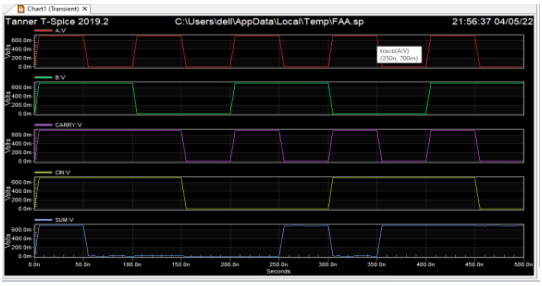

Fig 2 simulation results

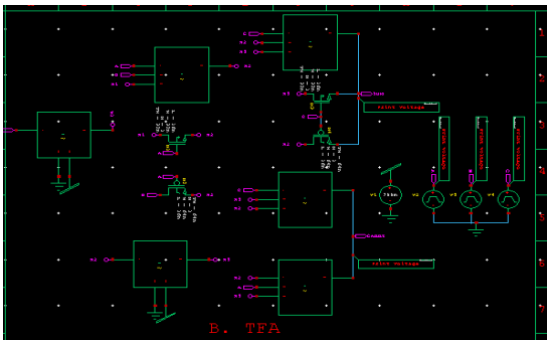

Fig 3 the ripple carry adder (RCA)

On a test bench comprised of a ripple carry adder (RCA) and a 6:2 compressor, carry and total output signals are subjected to multistage analysis. The RCA was chosen because its multi-stage route drive is well-suited to extracting the carry signal's timing characteristic. The 6:2 compressor, implemented in a five-stage cascade, has been chosen for capturing the temporal characteristics of the combined signal.

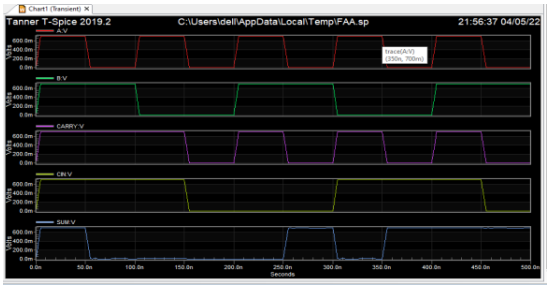

Fig 4. The time it takes for a circuit to transition from one state to another is referred to as "A. Switching Time."

What follows is a more in-depth look at the hybrid structure circuits that form the basis of the suggested logical effort analysis. A. Time to Alter When the output is linked to the buffer, the switching time of the circuits for two distinct input-output configurations is measured at a single test bench.

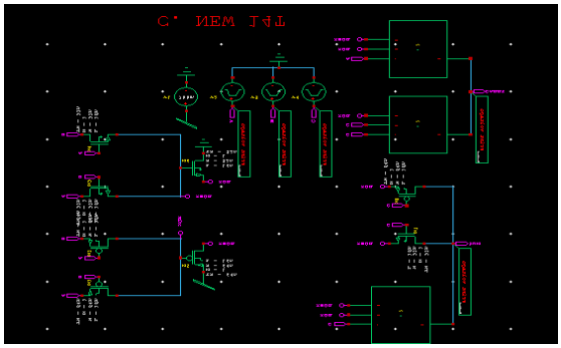

Fig 5. Driving skills Circuit drivability means the output can power the load.

Competence to Drive The drivability of a circuit is defined as the capability of the circuit's output to successfully drive a specified load. When the time it takes to charge the output capacitor is cut down, it becomes clearer that the circuit can provide a driving force.

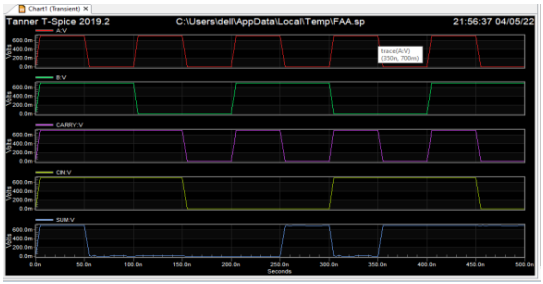

Fig 6:simulated waveform

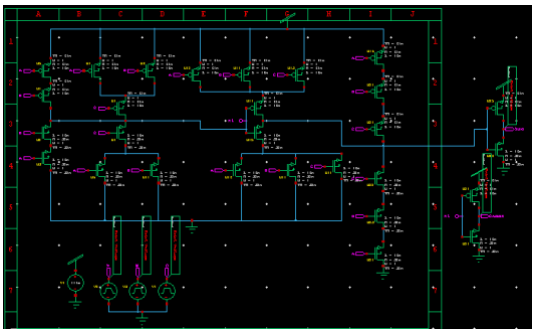

Fig7. Competence to Drive The drivability of a circuit refers to whether or not its output can successfully drive a specified load.

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Competence to Drive The drivability of a circuit is defined as the capability of the circuit's output to successfully drive a specified load. When the output capacitor charges faster, the circuit's driving power increases. The load capacitor is swept from 0 to 2 fF in 0.4 fF steps to measure the delay when the output is coupled to CL [Fig. 2(c)]. The capacitance of the load vs the delay line is then presented.

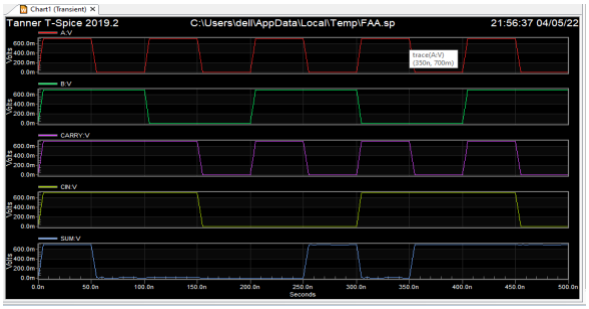

Fig 8 simulated waveform

Capacitance At Input The typical logical effort may be matched with the input capacitance, which is a crucial characteristic for timing analysis. On the test bed, the inverter is used to power the complete adder's inputs, and the sum and carry terminals are linked to variable-load capacitors of changing values. The input capacitance (Cin) is calculated as the physical value of the capacitor that creates the same delay [Fig. 1(f) and (g)].

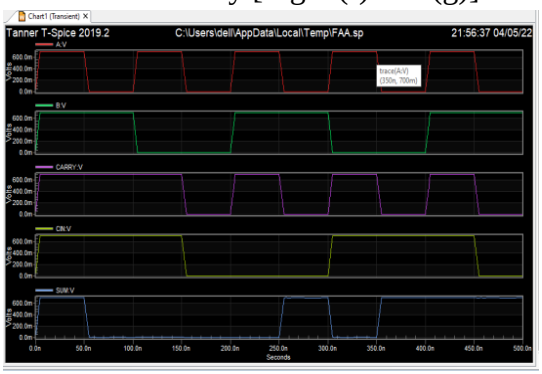

Fig 9:simulated waveform

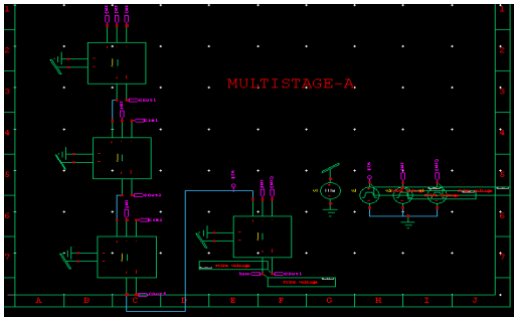

Fig 10: schematic of multistage

Gain If you want good results from a multistage design, you should aim for a low input capacitance and a high drive capability on a single test bench. A parameter called "gain" is used to estimate how well a multistage system works. It is the output drive capacity divided by the input capacitance.

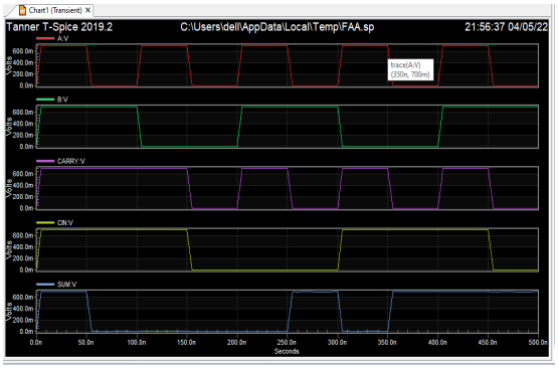

Fig 11: C-CMOS and New HPSC full adders feature parallel output delay lines.

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Power Results

VV1 from time 0 to 5e-07
Average power consumed -> 1.838148e-05 watts
Max power 2.385187e-05 at time 4.02976e-07
Min power 1.460557e-05 at time 3.05473e-07


Measure information will be written to file "C:\Users\dell\AppData\Local\Te

Measurement result summary
   tdealy         =   50.6508n
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V. CONCLUSION

In this work, we offer a novel logical effort analysis for adder circuits using a hybrid structure. We answer the question, "If hybrid full adders are faster

and use less energy and space than C-CMOS ones, How can a designer employ traditional logical effort to ensure multistage blocks are reliable? What parameters can they think about and control? For larger structures like giant adders, compressors, multipliers, etc., this 6study is necessary to evaluate the performance of the whole adders.

This paper illustrates how full adders react over time in terms of switching time, input capacitance, and output drivability. Model based on single test bench simulation results and multistage analysis. For circuits with more than one stage, it is possible to predict how the timing will work by measuring these three parameters, which can all be done on the same test bench. Gain, a novel metric defined as the ratio of output drivability to input capacitance, is a factor that might be adjusted by adjusting transistor size.

The Gain parameter allows the designer to regulate the circuit's power consumption and its output current. The selection factor is defined as the ratio of the Gain to the energy used, and it is presented here as a design and optimization parameter. In addition, a graphical categorization of hybrid cells is performed to reveal, at a glance, regardless of the circuit's complexity, which circuit is most likely to exhibit excellent performance. To validate the prediction analysis, HSPICE simulations are run on the adder cells and both CMOS 16nm technologies.

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