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Full Adder Using High performance 10T-XOR-XNOR Cell

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ABSTRACT

The design of an arithmetic circuitry mainly makes use of the new blended model. The strength of the circuit, holding duration, potential charge utility, and the efficiency of a complete adder all heavily influence how well the circuit operates. This project results in the construction of a ten-transistor logic circuit with high speed and low power consumption that simultaneously creates effective fluctuations and an output delay. Tanner software simulation employing 45nm technology is used to determine the performance efficiency of the planned circuit. The created circuit reduces the PDP factor over the pre-existing XOR-XNOR versions by at least 15%. Using the XOR-XNOR circuitry that has previously been created, as well as existing sum and carry generating blocks, we are presenting two distinct designs of complete adders in this project. In terms of power fluctuation product, the planned full adders provide improvements of between 10% and 40% over previous versions. The suggested full adders are installed in multistage full adder circuits to calculate the driving capabilities. The findings demonstrate that, among all the full adders, two of the developed full adders provide the best performance for a higher number of data bits. Keywords: PDP factor

I. INTRODUCTION

The folks of today are shown an interest in doing clever work to handle their routine activities without any time irregularities. Therefore, technological circuits draw people in. People are not only focused on the designing process; they are also considering how to do the task quickly and effectively. The size of the circuit, speed, and energy-efficient designs associated to those systems will be the designers' main design considerations [1].

The arithmetic circuits in electronic systems are heavily used to determine output efficiency. In essence, the summer serves as a foundational element for the many logical blocks. Most often, these circuits are used to transport data in related architectures [2]. Additionally, they are found in 1/3 of microprocessors that need electricity. to simultaneously enhance the overall look and the functionality of the adders.

We needed a few static CMOS logic models to be supplied in order to develop a complete adder. These logics may primarily be distinguished between two designing models: unblended and blended. The entire adder is created in a unit block using transistors in the traditional design procedure [3]. An example of this design approach is the terminating adder. In this circuit, the above and below portions of a complete adder are constructed utilising 24 active components.

It produces effective variable outcomes. The circuit's primary flaw is that it connects two N&P type transistors

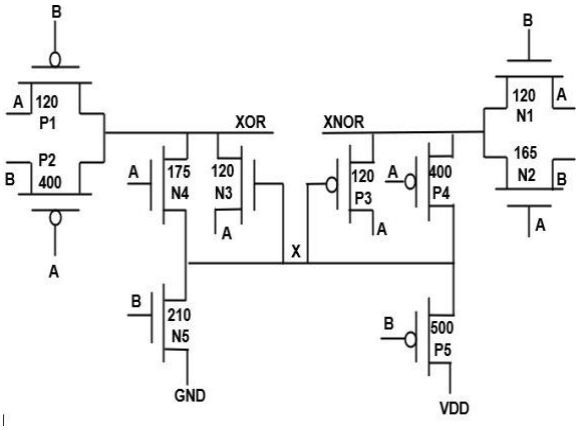
to a big forward capacitor, which may reduce the circuit's performance efficiency. Inverting moving transistor logic linked adders [4] and [5] are another design for the unblended model of the designing process.

This circuit's big speed multi stage, linked transistor type, and output reversing provide high speed and high swing output with great driving capacity. Due to the design's extensive usage of internal connections, there is a significant risk of loss. With the aid of differential transistors, we can create a complete adder [5]. The significant threshold voltage drop of differential transistors is a drawback. when the pair of N&P transistors' inputs are given the value "10." At the full adder, we did not get the same results. The input and output signals for these XOR-XNOR signals must be very strong.

People these days focus on new technology that can finish tasks faster and with better outcomes, and they also exhibit interest in working smarter to manage their daily activities without time inconsistencies. Therefore, technological circuits draw people in. People are not only focused on the designing process; they are also considering how to do the task quickly and effectively. The size of the circuit, speed, and energy-efficient designs associated to those systems will be the designers' main design considerations [1]. The arithmetic circuits in electronic systems are heavily used to determine output efficiency. In essence, the summer serves as a foundational element for the many logical blocks. Most often, these circuits are used to transport data in related architectures [2].

Additionally, they are found in one-fourth of all microprocessors. To simultaneously enhance the overall look and the functionality of the adders. A few prior works are being used as references for this endeavor. Having gained some fundamental information from such initiatives, we are preparing to create this sort of adder As the fundamental components of an adder, the authors employ transmission gates, pass transistors, and CMOS[1]-[3] logic gates. The authors focus on circuits that can provide results with little latency and little power consumption.

II .EXISTING METHOD



III. Existing system

In recent years, a number of XOR-XNOR circuit design strategies have been introduced and are reviewed in Section 1. Fig. 2 displays an XOR-XNOR circuit [13] that only requires six transistors to provide full swing outputs (a). The feedback restorer transistors and CPL logic are used to implement this configuration. It performs well in terms of delay for the AB inputs "01" and "10." However, there is a switching delay for the inputs AB: "11" and "00" at the output.

Naseri and Timarchi [15] overcome the problem of increased input latency by adding two nMOS and two

pMOS transistors to the circuit, as seen in Figure 2. (b). The latter design not only solves the issue of delayed response, but also minimizes the circuit's power usage. However, it requires an extra inverter since it uses input A.

In this part, a brand-new XOR-XNOR circuit is introduced that inverts the input inside, eliminating the need for an external inverter. This configuration reduces the number of internal nodes and transistors, hence reducing the XOR-XNOR circuit's total latency and power consumption.

Figure 3 depicts the proposed XOR-XNOR circuit with 10 transistors. (10-T). In XOR-CPL and cross-coupled architecture, XNOR is formed. Two pMOS (P1 and P2), three nMOS (N3, N4, and N5), four pMOS (P3, P4, and P5), and two nMOS (N1 and N2), three pMOS (N3, N4, and N5) transistors are on the XNOR output side (P3, P4, and P5). P1 and P2 are linked in parallel as PTL for XOR, while N4, N5, and N3 serve as feedback transistors and a restorer for full-swing output.

PTL, P4, and P5 transistors are coupled in parallel to give a full swing output, while P3 acts as a feedback transistor at the XNOR output side. This circuit generates XOR-XNOR outputs concurrently. Table I illustrates the charging and discharging channels for XOR and XNOR outputs. All output paths that create full and partial swing are provided. AB: "01" activates transistors P2, N1, and P4. While transistor P4 permits transistor P3 to pass "0" (-Vthp) at the XNOR output, transistors P2 and N1 pass "1" and "0" at the XOR and XNOR outputs.

AB: 10 activates transistors P1, N2, and N4. The weak logic "1" (VDD-Vthn) is transferred to the XOR output via transistor N3 and transistor N4. P1 and N2 pass "1" and "0" logic at XOR and XNOR outputs. Since full swing outputs have routes, the output swing for these inputs (AB: "01" and "10") will not be affected by weak logic outputs. AB: "00" activates transistors P1, P2, P4, and P5. P5 and P4 communicate complete logic "1" to XNOR and internal node X, whereas P1 and P2 send weak logic "0" (-Vthp) to XOR.

A logic "1" at node X activates transistor N3, which works when the XOR output is a strong logic "0." Similarly, the transistors N1, N2, N4, and N5 are activated when input AB is "11." However, transistors N4 and N5 discharge the XOR node fully. Furthermore, logic "0" is transferred to internal node X, activating transistor P3 and causing the whole logic "1" to be passed at the XNOR output.

IV. PROPOSED SYSTEM

The graphic depicts the simulation results for the Hybrid Full Adder-20 Transistor. The CMOS Tanner-SPICE Tool (Simulation Program with Integrated Circuit Emphasis) is used to simulate it. W- EDIT is used to investigate wave forms (wave form editor). A is 100 nm, B is 200 nm, and C is 300 nm, according to the simulation figure above. If A, B, and C are all equal to zero, so are the sum and the carry.

If A equals zero, B equals zero, and C equals one, the sum is one and the carry is zero. If A = 0, B = 1, and C = 0, the predicted total and carry is 1. If A0 equals 0 and B equals 1 and C equals 1, the sum is 0 and the carry is 1 If A equals 1, B

equals 0, and C equals 0, the sum is 1, and the carry is 0. If A equals 1 and both B and C equal 1, the sum is 0 and the carry is 1. If A equals 1 and both B and C equal 1, the total is 1 and the carry is 1 If A equals 1 and both B and C equal 1, the total is 1 and the carry is 1 If A equals 1, B equals 1, and C equals 1, the sum is 0 and the carry is 1.

Fig1: Schematic of proposed full adder Design

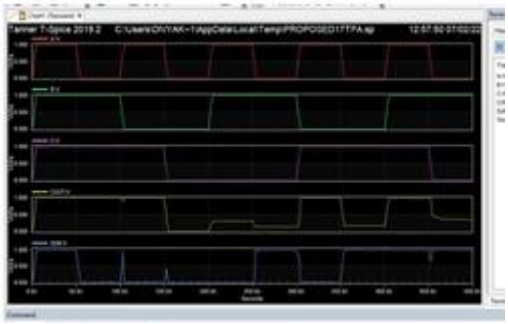


Fig2: Schematic results of proposed full adder Design

Fig3: Schematic of Full Adder Design 1 circuit

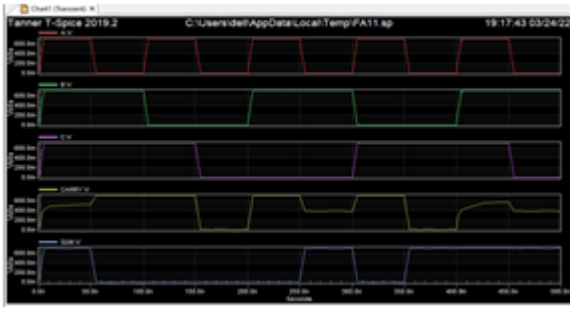


Fig4: Simulation results of Full Adder Design 1 circuit

The Hybrid Full Adder-20 Transistor simulation results are shown in the figure. The CMOS Tanner-SPICE Tool (Simulation Program with Integrated Circuit Emphasis) is used to simulate it.

W-EDIT lets you look into wave forms (wave form editor). Based on the simulation shown above, the carry will be "1" if A = 1, B = 1, and C = 0, the sum will be "0," and the sum will be "1," if A = 1, B = 1, and C = 1. A is 100 nm, B is 200 nm, and C is 300 nm. if A, B, and C are all zero, then the total is zero and the carry is likewise zero.

The total is "1" and the carry is "0" if A = 0, B = 0, & C = 1. Most likely, the total is "1" and the carry is "0" if A = 0, B = 1, & C = 0. A0= 0 and the carry will be 1 if B= 1 and C= 1 respectively. The total is "1" and the carry is "1" if A = 1, B = 0, and C = 0.

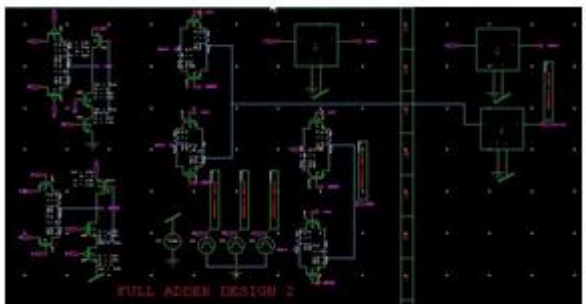


Fig 5: Schematic of Full Adder Design 2 Schematic

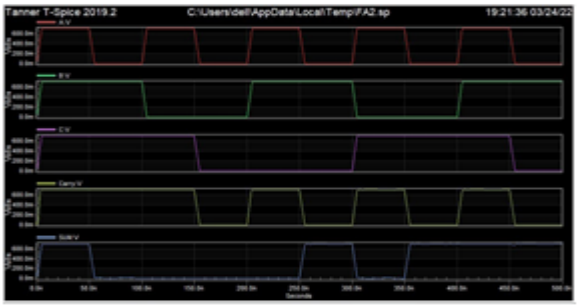


Fig 7: Simulation results of Full Adder Design 2 Schematic

The author proposed using a 6T XOR XNOR logic block circuit to build a standard full adder. This method demonstrated the use of two complimentary feedback boosters to reuse a signal with poor performance in differential mode when the logic of the two inputs was distinct. This circuit's outputs get their final voltage levels in two phases and have a significant delay for the same pair of logic value inputs.

Chang offers a solution to this issue. This suggested circuit produces improved driving capacity and output in full swing [13]. The XOR XNOR circuit at results is given an extra parasitic element by the X-coupled schematic. Table 1 shows a comparison of XOR and XNOR gates at full swing and half swing. There are several defaults in the change procedure that Naseri and Timarchi enhanced and were created for the 12T [14].

This circuit has a lower power need and provides a better delay. Further improvements have been made to the XOR-XNOR circuit's superior method of implementation. When we simulate that design using the Tanner 13 tool, we also discover several errors in the final circuitry. These shortcomings are seen as a problem by us in our project, and we are attempting to address them [14, 15].

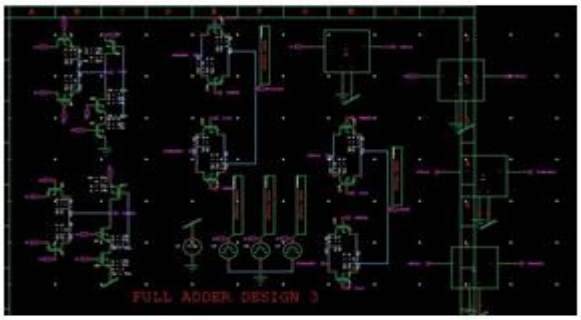


Fig 8: Schematic of Full Adder Design 3 Schematic

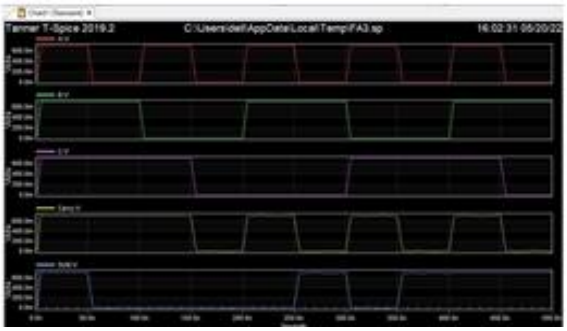


Fig 9: Simulation results of Full Adder Design 3 Schematic

V. Conclusion

This study led to the development of a novel 10-T XOR-XNOR circuit with simultaneous full swing outputs. Four more FA cells based on a hybrid logic design strategy and using the recommended XOR- XNOR circuit were also shown. How well the proposed XOR-XNOR circuit works and a FA cell was evaluated by simulating them in the 16nm CMOS technology of Mentor graphics. The latency and PDP of the suggested XOR-XNOR circuit were reduced by up to 65.16 and 70.13 percent, respectively, compared to those of previous designs. When compared to existing FAs, the suggested FA design-4 exhibited a PDP improvement of between 28 and 45 percent. In addition, the efficacy of the proposed FA cells was assessed using

cascaded connections. Among the existing FA cells, the suggested FA design-4 exhibited the highest performance for 2-bit and 4-bit cascading chains, while the proposed FA-3 exhibited the highest performance for 8-bit cascading chains.

VI. FUTURE SCOPE

Low power design is becoming more and more important in high-performance digital systems like microprocessors, digital signal processors (DSPs), and other applications. High clock frequencies emerge from the design of very sophisticated CPUs as chip density and operation speed increase. In order to lower the power in high-end systems with very high integration densities and hence increase operating speed, low power design is also necessary.

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