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Design and Implementation of High-Speed Hybrid Full Adder by Using 16nm

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ABSTRACT

Using transmission gates pass transistors, and conventional CMOS logic, a hybrid complete adder is created. The toolset for Mentor Graphics has been used to analyse the circuit's performance. Twenty-two (22) current Full Adder circuits have been examined with the performance parameters for comparative analysis a word length of 64 bits has also been put in place to test how well the proposed FA can grow. Only the proposed FA and five other designs can work without a buffer between phases when 64 bits are added. The entire adder being suggested, which uses only 17 transistors, the suggested design, which accounts for low power delay product, performs admirably in terms of power consumption and delay, according to simulation findings. The suggested hybrid FA circuit provides a compelling option in the data route design of contemporary high-speed Central Processing Units, according to the simulation findings. The proposed one bit full adder has been validated using Mentor 16nm Technology.

Keywords: Hybrid Full Adder Circuit, Pass Transistors, Transmission Gates, Conventional Complementary Metal Oxide Semiconductor.

I. INTRODUCTION

Research on low-power design of microelectronic circuits has substantially increased as a result of the fast expansion of transistor scaling. The need for high performance microelectronic circuit design has increased as a consequence [1]. A lot of math is used in modern image and video processing, digital signal processing (DSP) circuits, microprocessors, and many other applications [2]. The arithmetic operation of addition, one of the most fundamental, is employed extensively in modern computing systems.

One-bit Full Adders (FAs) are the cornerstone of most long-word arithmetic circuits, it is regarded as the core of binary addition [3–4]. As a result, enhancing FA performance is critical for improving A microprocessor's Arithmetic and Logic Unit (ALU) performance. In this work, an innovative hybrid FA is made up of PTs, TGs, and static CMOS circuitry.

The FA was built with 45 nm technology and Cadence tools. A comparison of the proposed design's performance characteristics with 20 already-existing FA devices with supply voltages ranging from 0.4 V to 1.2 V was done in order to assess the design's dependability. In order to verify the FAs' performance characteristics in large-scale circuits, they have also been expanded to broad word length adders.

In comparison to the current FA, the suggested FA demonstrated amazing performance in both single cell and extended form.

II. LITERATURE SURVEY

FA implementations using Complementary Pass Transistor Logic (CPL), 12 Transistor (12-T), and Conventional CMOS (CCMOS) logic all employ a single logic type. Voltage degradation requires additional buffers to restore CPL logic signals to source voltage. C-CMOS FA is independent to voltage degradation. C-CMOS FA has high input impedance. Researchers generally adopt a hybrid design technique that combines many logic models in one FA cell.

TGs are employed in the TGA and TFA adders [8, 9]. TGA and TFA FA are not affected by voltage decrease, but insufficient capability is. FA cells with 24, 14, and 10 transistors have different logic types. Instead of using two 2-input gates in a chain, the 24-T FA uses a 3-input XOR gate to figure out the sum. In 14-T and 10-T FA, the bits that are put in are XORed. The XOR gate's output generates the final output. 14-T and 10-T FAs have fewer transistors, reducing surface area. Driving ability limits its application in heavy fan-out circumstances. HPSC FA uses PTL to create XOR and XNOR signals in intermediate nodes. Outputs are full-swing using C-CMOS logic. CCMOS logic adds transistors and capacitance.

III. DESIGN, IMPLEMENTATION & RESULTS

BLOCK DIAGRAM OF EXISTING FULL ADDER

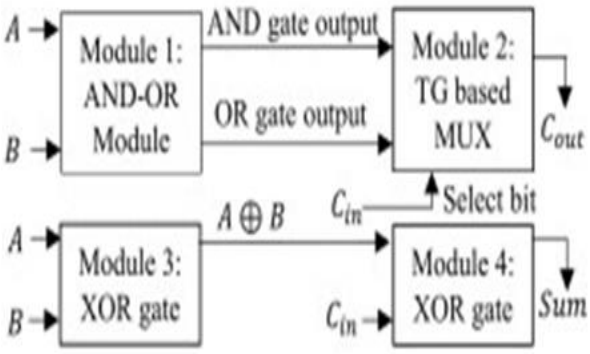

Figure 1: Block diagram of Existing full adder.

Post-layout simulation results for 0.4 V (the lowest voltage to prevent sub-threshold functioning), 0.8 V (the halfway value between 0.4 V and 1.2 V), and 1.2 V illustrate the effects of delay, power, and Power Delay Product (PDP) (normal operating voltage) 10-T FA may work at 180 nm with 1.8 V supply voltage. To compare, the 10-T FA has a power of 15.03 W and a delay of 129.48 ps. When the 12-T [6, 14-T, HPSC, and Hybrid 2 FAs were simulated with 0.4 V supply voltage, they did not work well. Further modelling with a 0.45 V to 0.75 V supply voltage established these FAs' lowest functioning voltages. 12-T [6], 14-T, HPSC, and Hybrid 2 FAs need 0.75 V, then 0.7 V, 0.7 V, and 0.5 V.

Additionally, it has been shown that when FA cells are working at a supply voltage lower than 0.8 V, delays begin to increase fairly dramatically. As technology advances, interconnect performance becomes increasingly dependent on resistance than capacitance. Resistance and capacitance must be re-optimized for best performance. Pan et al. show that expanding connection width beyond half pitch without modifying pitch improves VFET energy-delay product by 55% at 5nm.

Only five of the twenty existing FAs and the suggested design were found to function properly when expanded to 64 bits. According to Fig. 3, Hybrid 2, Hybrid 6, and GDI D1 FAs performed well in single cells. They can only be increased to a maximum of 8 bits in length; however this restriction occurs as a result of the signal's voltage decreasing as it propagates through several stages. The output signals for CCMOS [7] and 24-T FAs originate from VDD and GND since the output terminals use CCMOS-based logic.

As a consequence, each stage receives a new supply of voltage, which prevents voltage degradation in lengthy carry chains for CCMOS [7] and 24-T FAs.

SCHEMATIC DIAGRAM OF EXISTING FULL ADDER

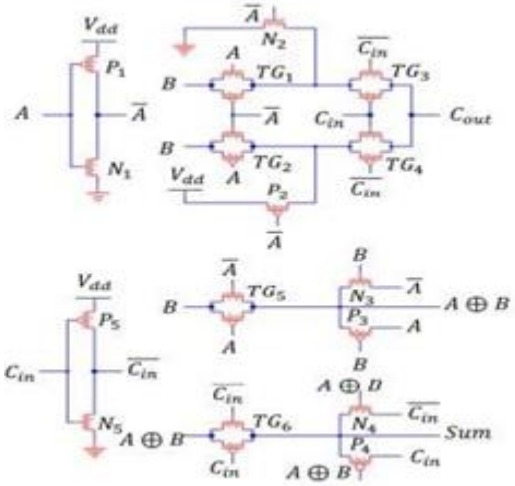

Figure 2: Schematic of the Existing Full Adder

IV. PROPOSED FULL ADDER WITH 17 TRANSISTORS

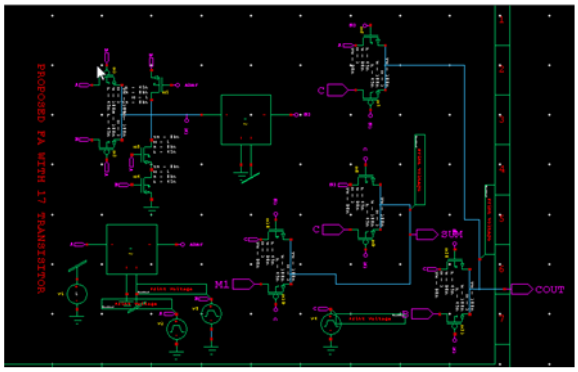

Figure 3: Proposed full adder with 17 transistors

The accompanying diagram represents the design of a hybrid full adder with 17 transistors, which is combinations of number of PMOS and NMOS logic is designed in 16nm technology .It is designed with tanner S-EDIT Tool. The following graphic depicts the simulation results for the hybrid complete adder-17-transistor. For simulation purposes, we employ CMOS Tanner-SPICE (Integrated Circuit Emphasis) Tool. W-EDIT is used to analyse wave shapes (wave form editor).

PROPOSED FULL ADDER SIMULATION RESULTS

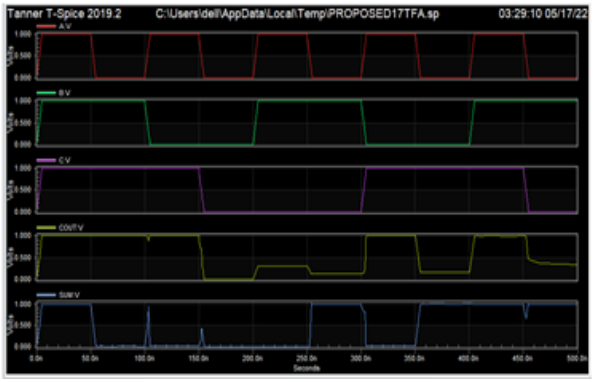

Figure 4: Proposed full adder simulation results

Based on the simulation picture above, assume that A is 100 nm, B is 200 nm, and C is 300 nm. If A, B, and C are all 0, then the total is 0 and the carry is likewise 0. The total is "1" and the carry is

"0" if A = 0; B = 0; & C = 1. Most likely, the total is "1" and the carry is "0" if A = 0, B = 1, & C = 0. A0= 0 and the carry will be 1 if B= 1 and C= 1 respectively. The total is "1" and the carry is "0" if A = 1, B = 0, & C = 0. If A = 1, B = 0, and C = 1, the total is 0 and the carry is 1, respectively. If A = 1, B = 1, and C = 0, the total is 0 and the carry is 1, respectively. The total is 1 and the carry is 1 if A = 1, B = 1, and C = 1.

Power Results

- VV1 from 0 to 5e-07 in time
- The typical amount of electricity used is 3.6985571e-07 watts.
- Maximum power at time 1.54624e-07,
- Minimum power at time 5e-08, and in between, 1.691323e-11

Power Analysis of Hybrid Full Adder-B-26Transistor

The power analysis of the Hybrid Full Adder-17 Transistor is shown in the above image. Tanner tool was used for the analysis. The average power use was 3.69 e-007 watts. Power maximum 1.03e-05 A minimum of 1.69e-11 watts of electricity was used. For the aforementioned simulation, 0.7 VDD was used.

Measurement result summary:

tdealy = 210.5680n

Delay Analysis of Hybrid Full Adder-17 Transistor:

The delay analysis of the Hybrid Full Adder-17 Transistor is shown in the above image. Tanner tool was used for the analysis. The time delay is 210.56n.For above simulation have done with 5 VDD.

Measurement result summary:

PDP = 291.1505

PDP Analysis of Hybrid Full Adder-17-Transistor:

The PDP analysis of the hybrid full adder-17 transistor is shown in the above image. Tanner tool was used for the analysis. The PDP is 291.1505. For above simulation have done with 0.7 VDD.

V. CONCLUSION

A unique hybrid FA design with noticeably better performance has been suggested in this study. Twenty FAs currently in use have been compared to the proposed design's characteristics. Utilizing the Mentor Graphics toolkit, simulation was done for performance analysis. According to simulation studies, the suggested FA exhibits improved performance when run as a single cell in terms of speed and PDP. The word length of FAs has also been raised to 64 bits to show scalability. When expanded to 64 bits, only the suggested FA and five of the conventional designs can operate without buffers between phases. The suggested architecture is better suited for the implementation of extended word-length adders in cascade mode, which is the current trend in computer systems that need to work quickly and use little power. In the proposed system, we used 16 nm to develop and construct a high-speed hybrid full adder, reducing the number of transistors from 22 to 17. Therefore, we may still minimize the number of transistors in the future. Then a few criteria, such as area, power consumption, and circuit design speed, vary with an appropriate outcome.

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