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# Exploring New XOR and XNOR Gates to Create a Low-Power and Quick Full Adder

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**ABSTRACT**

New circuits are suggested in this study for simultaneous XOR-XNOR and XOR/XNOR operations. There are considerable degrees of power use optimization in the proposed Circuits Short circuit output power loss is minimized, and output capacitance is kept to a minimum. We also offer six novel hybrid circuits for a 1-bit full-adder based on the unique full-swing gates that employ XOR-XNOR or XOR/XNOR (FA) (FA). Each suggested circuit offers benefits in terms of speed, power utilisation, power delay product (PDP), ability to drive, and other characteristics. To evaluate how well the suggested designs operate, a number of HSPICE and Cadence Virtuoso simulations are done. Based on the technology model for the 65-nm CMOS process, simulations demonstrate that the recommended designs are quicker and consume less power than alternative FA systems. Using a unique approach to transistor size, the PDP of the circuits is improved. The recommended technique rapidly determines the optimal value for the optimum PDP by using the numerical computing particle swarm optimization methodology. The modifications of the output capacitance, supply and threshold voltages, input noise immunity, and transistor size of the suggested circuit are all investigated.

**Keywords:** PDP (Power Delay Product), CMOS Technology, Cadence Simulations

## I. INTRODUCTION

Electronic devices are becoming a part of daily life in almost every aspect. Electronic systems are largely made up of digital circuits such as digital communication tools, microprocessors, and signal processors. The utility of circuits is limited as the degree of integration increases due to increased levels of power and space consumption. Due to the increasing need for and popularity of battery-operated portable devices like laptops, tablets, and mobile phones, designers are working to minimize the size and power requirements of these systems while maintaining their performance Optimizing .

W/L transistors may reduce a circuit's power-delay product (PDP) without generating supply voltage issues. Digital applications require adders, multipliers, and divisions. This study explores XOR/XNOR gate circuits and recommends novel layouts for both XOR/XNOR and simultaneous XOR/XNOR (XOR-XNOR) gates. Issues in the investigated circuits are also corrected.

The unique XOR/XNOR and XOR-XNOR circuits serve as the

foundation for six new FA architectures. What follows are the remaining sections of the article. There is an explanation of the XOR-XNOR and XOR/XNOR circuits. Simulation results for XOR/XNOR and XOR-XNOR circuits are available. The benefits and drawbacks of six novel FA circuits are shown and explored; all are based on the XOR/XNOR and XOR-XNOR gates.

## II. EXISTING SYSTEM:

In the present system, hybrid FAs consists of two modules: a 2-1-MUX gate and a 2-input XOR/XNOR (or simultaneous XOR-XNOR) gate. The bulk of the power in the FA cell is used by the XOR/XNOR gate. Consequently, by meticulously building the XOR/XNOR gate, the FA cell's power consumption can be decreased. The XOR/XNOR gate widespread use in the design of digital circuits.

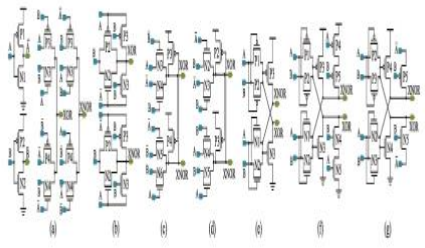

**Figure-1: Different types of XOR and XNOR approaches**

The full-swing XOR/XNOR logic gate circuit is shown in Figure (a) (DPL). Count eight transistors in this setup. Since NOT gates are needed to drive the output capacitance, their high power consumption on the critical path of the circuit is the main drawback. So, to shorten the critical route delay, the transistor size in the NOT gates should be increased. Figure 2 is yet another illustration of a six-transistor XOR/XNOR full-swing gate (b).

This circuit's latency and power usage are based on PTL logic are superior than those of the circuit shown in Fig(a).Using a NOT gate on the circuit's crucial route is the only issue with this construction

In XNOR, the critical path consists of NOT gates and a pMOS transistor (P5) (pMOS transistor is slower than nMOS transistor). Quicken the XNOR circuit by increasing the size of the pMOS transistor (P5) and the NOT gates. On display in Figure 1 is an XOR-XNOR logic circuit (c). This circuit uses CPL logic and is: the usage of ten transistors The outputs in this arrangement are controlled by nMOS transistors. Inputs AB = 00 in Figure (d) cause transistors N3, N4, and N5 to go into their "off" states, thereby sending the logic "0" to the XOR output.

With XOR set to 0, the XNOR output of transistor P3 will be charged to VDD. Therefore, the critical path in this circuit is much longer than in the circuit shown in Fig (c). The six-transistor full-swing XOR-XNOR gate depicted in Fig. (e) is shown. The output node's weak logic is restored by the N3 and P3 feedback transistors, which are complementary (XOR and XNOR).

## III. PROPOSED SYSTEM

The XOR/XNOR circuit shown in Figure 2(a) is power and latency efficient. Similarly, this arrangement has a problem with output voltage drop for a single logical input value. We suggest the circuit shown in Fig. 2 to address this issue and offer the XOR/XNOR gate its ideal shape2 (b). This structure's output is in full swing for all possible input configurations. The

crucial route of the circuit for the suggested XOR/XNOR gate lacks NOT gates. Consequently, compared to the structures in Fig2 (a) and Fig2(b), it will have a reduced latency and better driving capabilities.

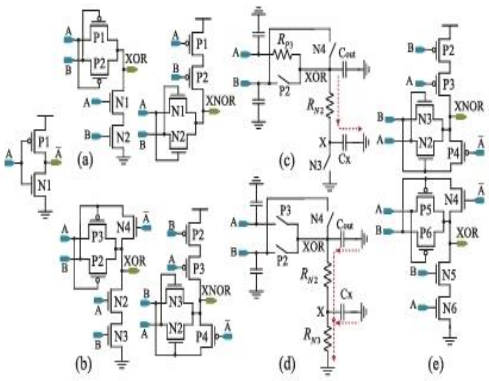


**Figure-2: Hybrid Full Adder circuits**

The recommended XOR/XNOR gate has one more transistor than the configuration in Fig. 2(b), but it runs more quickly and efficiently. Fig. 2 depicts the suggested 12-transistor simultaneous XOR-XNOR gate arrangement (e). This architecture results from combining the two recommended XOR and XNOR circuits of Fig. 2(b). In this instance, the power and delay are optimized, and the input capacitances are roughly equal. This structure's output capacitance is very low, and there are no NOT gates on the critical path. It is therefore extremely fast and uses little power. The output delays of this circuit's XOR and XNOR are almost identical, which reduces jitter in the step that follows.

This circuit's other advantages are its full-swing output, high supply voltage resistance, and resistance to transistor size scaling. Comparing XOR/XNOR and simultaneous XOR-XNOR structures. The 1 GHz inputs were linked to a 4-unit inverter (FO4) (as a load). Using the offered transistor sizing technique, the ideal PDP transistor size was calculated. The suggested procedure will be presented. PDP is determined by dividing worst-case delay by main circuit power consumption.

The XOR and XNOR structures outperform equivalent ones.

The proposed XOR and XNOR circuits have the lowest PDP and latency. These two proposed circuits' close proximity in terms of latency also prevents glitches from developing at the following level. the XOR and XNOR circuits' latency, power usage, and PDP. For varied applications six novel FA circuits that we suggested are shown in Fig. 6.

The schematic diagram of the suggested FA cell. All of these new FAs were made with the XOR/XNOR or XOR-XNOR circuit, which was already mentioned and they were all implemented utilising a hybrid logic strategy. The hybrid FA cells presented employ the well-known four transistor 2-1-MUX arrangement. The HFA-20T and HFA-17T circuits were intended to use the fewest available transistors. To make just the C signal, you use the output Sum signal, the XOR, and the XNOR. You don't need any extra NOT gates for this.

Yet if the Sum output is likewise made using the C signal, so the Sum output won't be driven by the XOR and XNOR signals only they will be connected via the TG multiplexer to the 2-1-MUX data-select lines. Hence, the XOR capacitance XNOR nodes shrink, the circuit latency increases, and will be enhanced.

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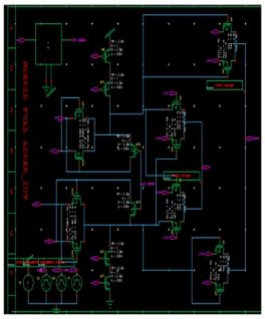
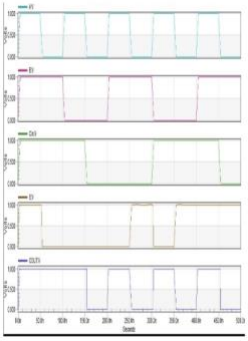
**COMPARISION TABLE OF EXISTING AND PROPOSED SYSTEM:**

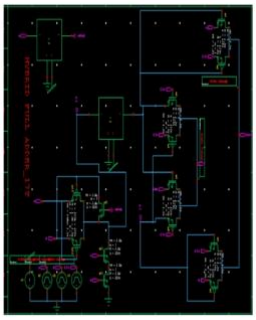
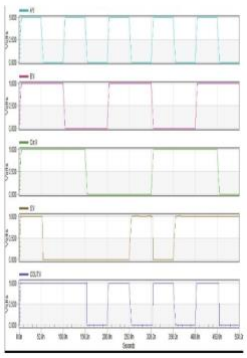
| Design names | Existing Technology with 65nm | | | Proposed Technology with 16nm | | |
|---|---|---|---|---|---|---|
| | Power (W) | Delay (ns) | PDP | Power (W) | Delay (ns) | PDP |
| Design-A | 10.46 | 55.8436 | 340.9870 | 6.31 | 48.43n | 305.8782 |
| Design-B | 7.98 | 190.8456 | 805.7815 | 4.86 | 149.7216 | 728.7686 |
| Design-C | 3.69 | 210.5680 | 291.1505 | 1.4 | 151.4230 | 223.3075 |
| Design-D | 3.69 | 210.5680 | 291.1505 | 1.4 | 151.4230 | 223.3075 |
| Design-E | 3.69 | 210.5680 | 291.1505 | 1.4 | 151.4230 | 223.3075 |
| Design-F | 3.69 | 210.5680 | 291.1505 | 1.4 | 151.4230 | 223.3075 |

## IV. RESULT

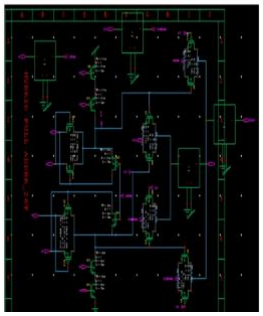
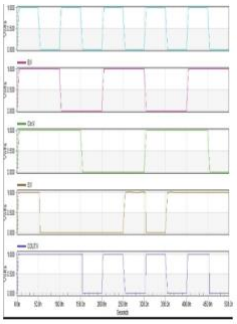
Based on the simulation results, the proposed HFA-22T cell could cut PDP and EDP by up to 23.4% and 43.5%, respectively, compared to its strongest competitor. At all voltages of supply between 0.65 V and 1.5 V, this cell is more powerful and quicker than its predecessors. The suggested HFA-22T is quicker and more energetic at every process corner when compared to previous FA designs. Normally, all indicated FAs are responsive to PVT changes. Schematic Design of HFA-20T

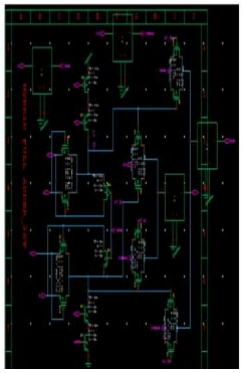
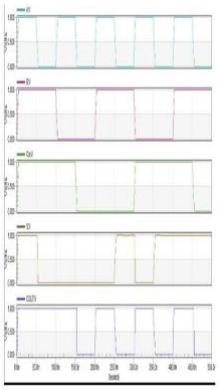
Schematic Design of HFA-17T

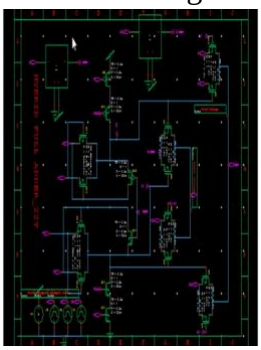
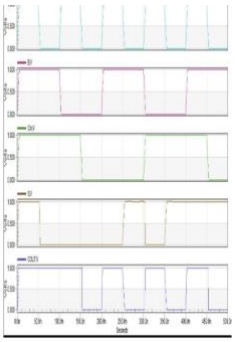
Schematic Design of HFA-B-26T

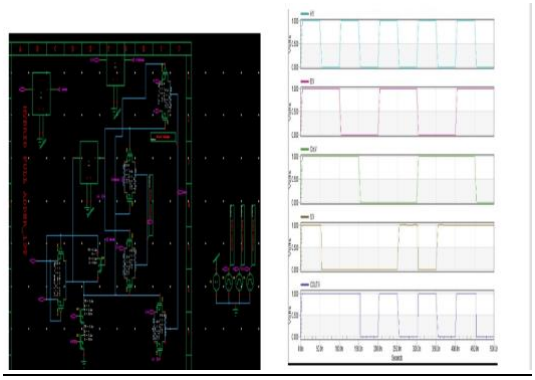
Schematic Design of HFA-NB-26T

Schematic Design of HFA-22T

Schematic Design of HFA-19T



## V. CONCLUSION

The XOR/XNOR and XOR-XNOR circuits were originally evaluated in this study. The results of the research demonstrated that using NOT gates on a circuit's critical route had drawbacks. Another flaw in a design is the lack of positive feedback for altering the output voltage level on the XOR-XNOR gate outputs. This feedback raises the circuit's energy consumption by increasing the delay and output capacitance. Next, we included new XOR/XNOR and XOR-XNOR gates without the drawbacks.

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